Figure 6 Comparison of the f_T versus I_C performance for HBT with and without Zn diffusion process. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

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A K-BAND LOW-NOISE AMPLIFIER IN 0.18-μm CMOS TECHNOLOGY FOR SUB-1-V OPERATION

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ABSTRACT: A K-band low-noise amplifier (LNA) was realized in a standard 0.18-μm CMOS technology. The cascaded common-source configuration of four stages was adopted for low voltage operation and high gain performance. In addition, the gate-source transformer feedback technique was employed to achieve a low noise figure (NF), which also enabled a single power supply operation and without using any resistive components. Under a supply voltage of only 0.8 V and a DC power consumption P_{DC} of 12.6 mW, the measured gain and NF are 14.5 and 5.3 dB at 21 GHz, respectively. © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 2202–2204, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop. 24530

1. INTRODUCTION

The increased demands on data capacity have pushed the operation of wireless communication systems towards a higher frequency range. One of the key building blocks in wireless communication systems is the low-noise amplifier (LNA) which determines the sensitivity of the receiver. Various techniques have been proposed for LNA design to achieve low noise figure (NF) and high gain [1–6], while a main challenge is to maintain good performance under a low operation voltage and a low power consumption. Many CMOS LNAs operated at K-band (18–26 GHz) have been reported [7–10]. However, none of these circuits was operated below 1 V and by a single power supply.

In this work, we demonstrate a high-performance LNA for sub-1-V operation with a cascaded common-source (CS) and inductive-component-only configuration. Using feedback transformers and matching inductors, the LNA realized in a 0.18-μm CMOS technology achieves a gain of 14.5 dB and a NF of 5.3 dB at 21 GHz under a single supply voltage of only 0.8 V and a corresponding power consumption of 12.6 mW.

2. LNA DESIGN

Figure 1 shows the circuit configuration in this design. Four cascaded CS stages are used to achieve a high-gain characteristic. For a low voltage operation, only inductive components are employed. The inductors $L_1 \sim L_4$ are connected to the drain of the transistor directly. The bias voltage V_{DD} can be minimized because there is no extra DC voltage drop and the effective RF voltage at the drain terminal can exceed V_{DD}. With the transformers ($T_1 \sim T_4$), the supply voltage can also be applied directly to the gate terminals for a low-voltage operation. As can be seen, the overall bias scheme of this design only requires one supply voltage and without any resistive components. In addition, for a better power and noise matching simultaneously, the transformer feedback technique [4–5] is employed between the gate and source of the MOSFET in each stage. For a simple CS stage, the main noise source is the channel noise current of the transistor, which can be referred to the input as a noise voltage source by dividing the transconductance of the device. By adding a transformer as shown in Figure 1, the negative feedback path creates a correlated noise voltage source at the input node but with a 180° phase difference. As a result, the noise voltage is partially canceled, and the overall NF is reduced. For the transformer designed to achieve a low NF, the quality factor Q is critical. By considering Q of the transformers, the designed turns ratio n and coupling coefficient k are optimized to 1.54 and 0.35, respectively, and L_P and L_S are designed as 0.3 nH and 0.13 nH, respectively. Also, by considering the geometry of the transistor (a total gate width of 48 μm) together with the primary L_P and secondary L_S inductances, an input impedance of 50 Ω can be achieved.

The interstage matching is also considered to ensure the circuit stability and achieve an excellent power gain in the cascaded
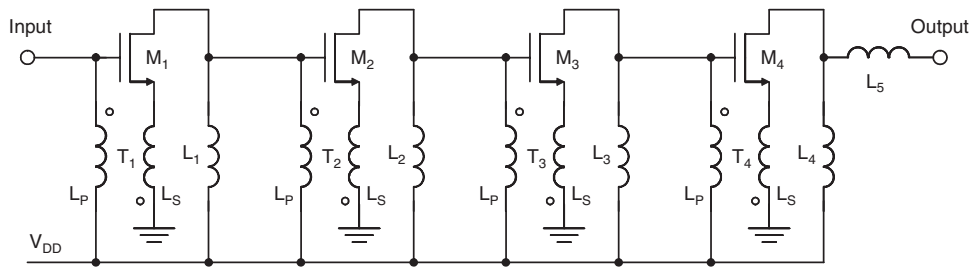
Figure 1 Circuit topology of the proposed K-band LNA

topology. For simplicity, both the input and output impedances of each stage are designed to be 50 Ω. As mentioned, the input matching is codesigned with the feedback transformer. On the other hand, the output matching is achieved using the shunt inductors $L_1 \sim L_4$. Note that these inductors also function as a parallel LC resonant network to cancel the parasitic capacitance at the drain node. In addition, they act as load and RF choke simultaneously. To simplify the design, four identical CS stages with the transformer feedback are cascaded directly. However, even with slight impedance mismatch in each stage owing to the parasitics in the actual layout, the cascaded configuration resulting in increased deviation from 50 Ω of the overall output. Therefore, the inductance of L_2 and L_3 is reduced and an additional inductor L_5 is connected in series at the output node for better output matching in the final design. The EM simulator was used to obtain the RF characteristics of the inductive components.

3. RESULTS AND DISCUSSION

The proposed LNA was fabricated in a standard 1P6M 0.18-μm CMOS technology. The chip area including DC and RF probing pads is 0.7×0.55 mm^2 (core area: 0.6×0.28 mm^2), as shown in Figure 2. Special care was taken for the chip layout, in which the semicoaxial line structure was adopted to alleviate the RF loss from the Si substrate and crosstalk through SiO$_2$ or Si layers [11]. The S-parameters were measured from 10 to 40 GHz, as shown in Figure 3. Under a single supply voltage of only 0.8 V (DC power consumption P_{DC}: 12.6 mW), a peak gain S_{21} of 14.5 dB is observed at 21 GHz and the -3-dB bandwidth is from 19.1 to 23.8

GHz. The S_{11} and S_{22} are -15.4 and -13.4 dB at 21 GHz, respectively. The reverse isolation S_{12} is well below -30 dB within the unit-gain bandwidth. Under the same bias condition, the NF is 5.3 dB at 21 GHz and the lowest value achieved is 5.2 dB at 23.5 GHz, as shown in Figure 4. Compare to the simulated results, the operation frequency is dropped ~3 GHz and the NF is 0.8 dB higher which may be attributed to undesired parasitic effects and also the inaccuracy of the active device model. The output power was measured as a function of the input power at 21
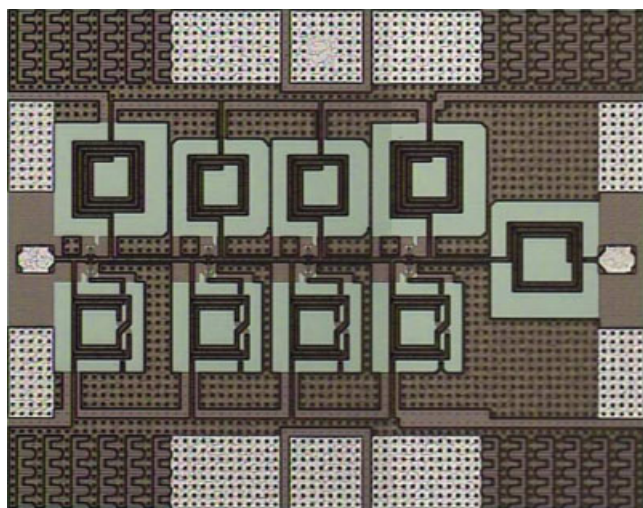

Figure 3 Simulated and measured S-parameters

Figure 2 Chip micrograph. (Chip area: 0.7×0.55 mm^2, core area: 0.6×0.28 mm^2). [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]
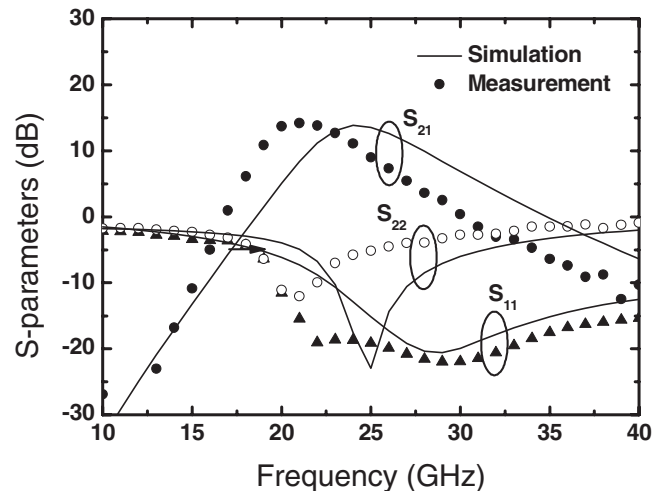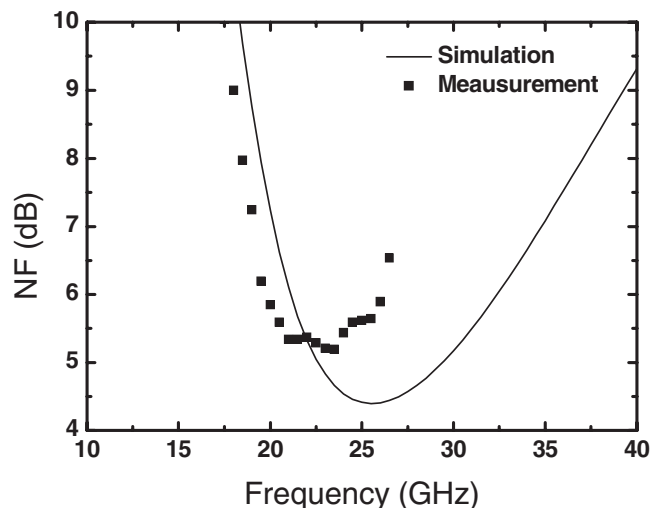

Figure 4 Simulated and measured NF as a function of frequency

TABLE 1 Comparison of K-Band CMOS Amplifiers

Ref.	This Work	[7]	[8]	[9]	[10]
Freq. (GHz)	21	21.8	23.7	24	20
Gain (dB)	14.5	15	12.9	13.1	9
NF (dB)	5.3	6	5.6	3.9	5.5
BW (GHz)	4.7	—	—	4	5.3
S_{11} (dB)	−15.4	−21	−11	−15	−9
S_{22} (dB)	−13.4	—	−22	−20	−14
$P_{1dB,ln}$ (dBm)	−14.5	—	−11.1	−12.2	−10
Voltage (V)	0.8	1.5	1.8	1	1.2
Power (mW)	12.6	24	54	14	24
Chip area (mm²)	0.7 × 0.55	—	1.05 × 0.7	0.57 × 0.6	0.8 × 1
CMOS technology	0.18-µm	0.18-µm	0.18-µm	0.18-µm	0.13-µm

GHz. The obtained input 1-dB compression point $P_{1dB,in}$ is −14.5 dBm.

The circuit performances are summarized in Table 1 together with the recently reported K-band CMOS amplifiers [7–10] using similar or more advanced technologies. Compared with these amplifiers, this work demonstrates a comparable RF performance under the lowest operation voltage.

4. CONCLUSION

A sub-1-V 21-GHz LNA was successfully demonstrated in a standard 0.18-µm CMOS technology. The chip area including the DC and RF probing pads is 0.7×0.55 mm² (core area: 0.6×0.28 mm²). By the CS cascaded configuration, this design employed only inductive components for feedback and matching purposes to achieve high gain and low voltage operation simultaneously. Under a single supply voltage of 0.8 V and a power consumption of 12.6 mW, the proposed LNA demonstrated a NF of 5.3 dB with an associated gain of 14.5 dB.

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MICROWAVE CHARACTERISTICS OF SUBSTRATE INTEGRATED WAVEGUIDE PHOTODETECTOR

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ABSTRACT: *In this article, using a novel structure, simulated and measured microwave characteristics from substrate integrated waveguide photodetector (SIWPD) are obtained and compared with the conventional microstrip waveguide photodetector. A Ka-band microstrip to rectangular waveguide multilayer transition for OC-768/STM-256 optical systems is designed and fabricated. Attenuation constant results shows that by replacing substrate integrated waveguide (SIW) instead of conventional microstrip in waveguide photodetectors, operation frequency can be increased. Microwave fields in the proposed structure show a good transition from quasi-TEM mode to TE_{10} mode in multilayer structure. The multilayer structure is considered to separate SIW and DC bias of the photodetector.* © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 2204–2207, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24528

1. INTRODUCTION

Waveguide photodetector (WGPD) is one the key components for optical communication systems. WGPD as a two port device with optical input and microwave output is the type of edge illuminated photodetectors [1]. Optical input power and bandwidth of such devices can be increased comparing the surface illuminated photodetectors.

Microwave characteristics of a long traveling wave photodetector which is one type of WGPDs for high-power operation are discussed in [2]. In this article, attenuation constant increases by frequency and so they are not applicable for high frequencies.

In Ref. 3, 20 GHz of bandwidth for a WGPD without bias in 1550 nm is obtained. Also, microwave loss analysis and measurement of lossy microstrip line in GaAs optical substrate used in WGPD structure are carried out in [4, 5]. In WGPD, bandwidth is limited by detection and transmission parts. Long length of the microstrip transmission part has a significant role in the bandwidth limitation of WGPD and may be replaced by low loss microwave waveguide. Rectangular waveguide with the low value of microwave loss is a good candidate. Two problems are expected by replacing rectangular waveguide instead of the microstrip line in the transmission part of WGPD. First is related to the cutoff frequency of RWG. To solve this problem, new WGPDs can be