A 75-dB · Ω 10-Gb/s Transimpedance Amplifier in 0.18-μm CMOS Technology

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***Abstract*—A six-stage transimpedance amplifier (TIA) was realized in a 0.18-μm complementary metal–oxide–semiconductor process. By adopting an effective gain-bandwidth product (GBW) enhancement technique, π-type inductor peaking, the measured S_{21}, transimpedance gain, and bandwidth are 41 dB, 75 dB · Ω, and 7.2 GHz, respectively, in the presence of an on-chip photodiode capacitance of 450 fF at the input. The 10-Gb/s TIA can operate under a maximum output swing of 800 mV_{pp} and achieve a recorded GBW per DC power of 441.1 GHz · Ω/mW.**

***Index Terms*—Complementary metal–oxide–semiconductor (CMOS), gain-bandwidth product (GBW), inductor peaking, photodiode, transimpedance amplifier (TIA).**

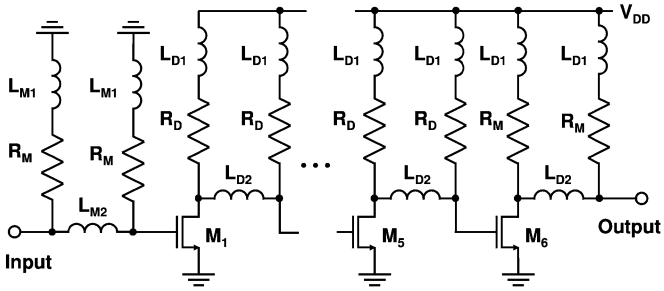

Fig. 1. Circuit topology for the 75-dB · Ω 10-Gb/s TIA.

I. Introduction

THE FIRST gain stage of an optical–electrical receiver is the transimpedance amplifier (TIA), which converts the small input current into a large output voltage [1]. The main design issues include circuit sensitivity, transimpedance gain, operation speed, and output voltage swing [2]–[6]. In addition, a good design should feature a high gain-bandwidth product (GBW) per DC power $(\mathrm{GBW}/P_{\mathrm{DC}})$ to relax the design specifications of other circuit blocks in the receiver chain. Many GBW enhancement techniques have been proposed for high-performance TIAs using 0.18-μm complementary metal–oxide–semiconductor (CMOS) technology [7]–[10]. Among them, the maximum transimpedance gain (Z_T) achieved was 62.3 dB · Ω using the technique of shunt-inductor peaking [7]. The highest $\mathrm{GBW}/P_{\mathrm{DC}}$ achieved was 115.1 GHz · Ω/mW by using series-inductor peaking [8].

In this letter, a 75-dB · Ω TIA with an output voltage swing of 800 mV_{pp} is demonstrated by employing a more effective GBW enhancement technique, π-type inductor peaking (PIP) [11], [12]. The proposed TIA presents the highest Z_T among the published results using CMOS technology for 10-Gb/s applications. With an operation speed of 10-Gb/s, a recorded $\mathrm{GBW}/P_{\mathrm{DC}}$ of 441.1 GHz · Ω/mW is achieved.

This letter is organized as follows. Section II presents the details of the proposed TIA including the design for the multistage amplifier and the PIP technique. The measured results are shown in Section III, and Section IV concludes this work.

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II. TIA Design

Fig. 1 shows the proposed circuit topology of the TIA. The common-source (CS) stage in cascade is adopted to produce a high Z_T. The CS configuration was chosen owning to the low bias voltage allowed comparing with the commonly used cascade topology for high-frequency design. In addition, the PIP inductors can create two zeros and two pairs of complex conjugate poles in the transfer function resulting in significantly enhanced bandwidth [12]. Note that the PIP topology only alters the frequency response, whereas the DC power consumption remains unchanged compared to the basic CS amplifier without the PIP inductors. As a result, the proposed approach can achieve a remarkable $\mathrm{GBW}/P_{\mathrm{DC}}$ value. For a cascaded amplifier with identical first-order gain stages, the optimal stage number (n_{opt}) to achieve a maximized circuit bandwidth can be estimated by a simple equation of $2 \times \ln(A_{\mathrm{tot}})$, where A_{tot} is the total voltage gain [13]. Note that A_{tot} is equivalent to the overall S_{21} under the matched input and output impedances of 50 Ω. For the proposed TIA with an A_{tot} of 41 dB (75 dB·Ω), the calculated n_{opt} is 9. Under a fixed bandwidth of about 7 GHz for the 10-Gb/s operation, the nine-stage design has a large GBW but also consumes a huge P_{DC}. We observe a trend by simulation that $\mathrm{GBW}/P_{\mathrm{DC}}$ increases with the reduced stage number owing to a faster reduction rate of P_{DC} than that of the gain. This trend keeps until a maximum $\mathrm{GBW}/P_{\mathrm{DC}}$ achieved with a stage number of 6 in our design. As the stage number continuously reduces, the trend reverses (gain drops faster than P_{DC}) and thus $\mathrm{GBW}/P_{\mathrm{DC}}$ reduces. Consequently, the finally designed stage number is 6 with a P_{DC} of 91.8 mW.

To increase the GBW of each gain stage, the PIP technique with three peaking inductors is employed. The concept of PIP $(L_1 \sim L_3)$ is illustrated by the small-signal circuit model of

TABLE I
COMPARISON OF THE STATE-OF-THE-ART TIAS IN 0.18-μm CMOS/BICMOS TECHNOLOGY

Ref.	This work	[7]	[8]	[9]	[10]
Z_T (dBΩ)	75.0	62.3	61.0	54.0	52.0
BW (GHz)	7.2	9.0	7.2	9.2	7.6
Data Rate (Gb/s)	10	10	10	10	7.5
C_{pd} (fF)	450	150	250	500	0
Sensitivity	-16.4 dBm	—	10 μA	-18 dBm	-19 dBm
V_{DD} (V)	1.8	1.8	1.8	2.5	2.0
P_{DC} (mW)	91.8	108.0	70.2	137.5	34.0
GBW/P_{DC} (GHzΩ /mW)	441.1	108.6	115.1	33.5	89.0
Chip area (mm^2)	1.35x0.69	—	0.14	0.8x0.8	0.84x0.61
Process	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm BiCMOS	0.18μm CMOS

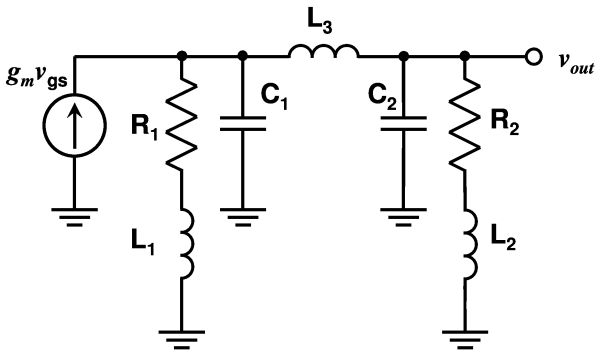

Fig. 2. Small-signal circuit model of a CS stage with PIP ($L1 \sim L3$).

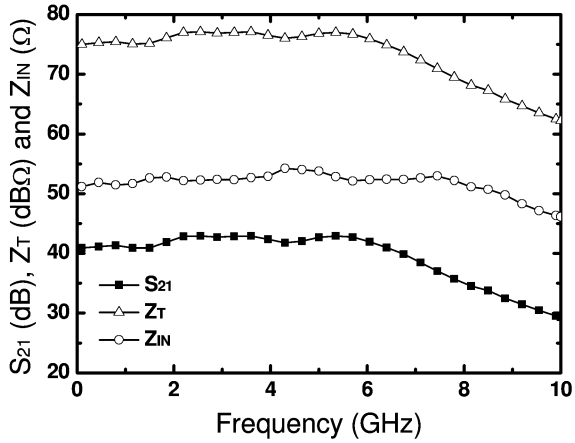

Fig. 3. Measured S_{21}, Z_T, and $Z_{\rm IN}$.

a CS stage as shown in Fig. 2. Without considering the inductors, the GBW $(g_m/2\pi(C_1+C_2))$ of this circuit is limited by the equivalent drain capacitance C_1 and the load capacitance C_2, where C_2 describes the equivalent gate capacitance of the next stage in a cascaded CS topology and g_m is the device transconductance. The ratio of C_2 to C_1 is around 3 for an RF N-MOSFET in a 0.18-μm CMOS technology [11], [12]. By inserting L_3, as can be seen, C_1, C_2, and L_3 form a third-order low-pass filter. The drain resistors R_1 and R_2 can be treated as the source and load resistors of the two-port network, and designed to be equal for impedance matching between different stages. Theoretically, the GBW of this two-port network can be maximally enhanced up to $2g_m/\pi C$ if $C_1 = C_2 = C/2$ [9], and the resulted bandwidth enhancement ratio (BWER) is 4. However, the imbalance between C_1 and $C_2(C_2 = 3C_1)$ causes the third-order filter to be asymmetric, which degrades the expected BWER to be 2.15. By inserting two more shunt-peaking inductors (L_1 and L_2) in series with R_1 and R_2, the BWER can be further improved by resonating with C_1 and C_2 in parallel. Based on the transfer function of the RLC low-pass filter, the required inductances can be estimated as: $L_1 = 0.8R_1^2C_1$, $L_2 = 1.5R_1^2C_1$, and $L_3 = 0.86R_1^2C_1$, and a BWER of 3.31 can be obtained for a CS stage without disturbing the low frequency gain [11], [12].

To accommodate the PIP inductors (L_{M1}, L_{M2} and L_{D1}, L_{D2}) in each gain stage, two matching resistors R_M and two drain resistors R_D are adopted. The input $(Z_{\rm IN})$ and output impedances are both matched to 50 Ω through R_M. With a resistor R_D of 200 Ω, the drain voltage of $M_1 \sim M_5$ is biased to be $V_{dd}/2$. The gate width of $M_1 \sim M_5$ is designed as 80 μm, while that of M_6 is enlarged as 96 μm to increase the driving capability and the output voltage swing. Based on the equations shown above for the initial values and the assistance of the CAD tool, the finally employed PIP inductances are as follows: $L_{M1} = 1.5$ nH, $L_{M2} = 1.6$ nH, $L_{D1} = 4.0$ nH, and $L_{D2} = 0.5$ nH. Although is not shown in the figures, the simulated results confirm that the TIA with PIP shows an overall improvement of 7.4 × in bandwidth compared to that without any bandwidth enhancement technique in this design. In addition, a GBW/$P_{\rm DC}$ improvement of 7.4 × can also be obtained since the DC power remains unchanged in the PIP configuration.

III. MEASUREMENT RESULTS

The TIA was measured on-wafer by the ground–signal–ground probes for S-parameters and transient measurements. From the measured S-parameters, the S_{21}, Z_T, and $Z_{\rm IN}$ are 41 dB, 75 dB · Ω, and 51 Ω at low frequencies, as shown in Fig. 3. The 3-dB bandwidth of Z_T is 7.2 GHz in the presence of an on-wafer $C_{\rm pd}$ of 450 fF at

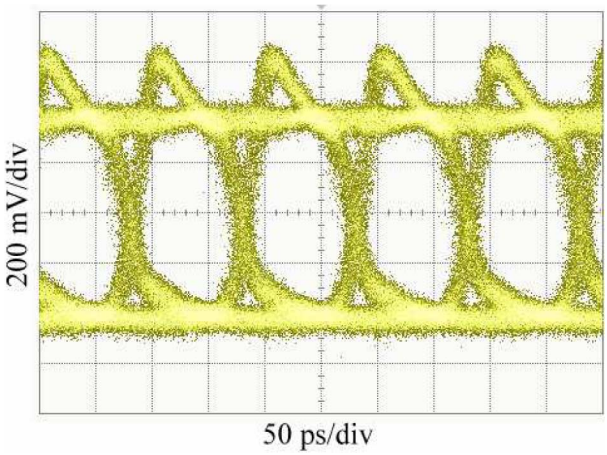

Fig. 4. Measured eye diagram for 10-Gb/s 231-1 PRBS at 400 μA_{pp}.

the input. Note that C_{pd} is used to account for the photodiode parasitic capacitance, which should be applied for practical TIA design consideration. A 10-Gb/s $2^{31}-1$ pseudorandom binary sequence (PRBS) is used to measure the transient response of the TIA. For an input current of 400 μA_{pp}, the eye diagram of the TIA with PIP is shown in Fig. 4. The measured maximum output voltage swing is around 800 mV_{pp}. From the measured bit-error rate (BER), the extrapolated sensitivity at a BER of 10^{-12} is -16.4 dBm. The circuit consumes a DC power of 91.8 mW from a 1.8-V power supply, and demonstrated a GBW$/P_{DC}$ of 441.1 GHz $\cdot\ \Omega/$mW. The circuit performances of the proposed TIA with the PIP configuration are summarized in Table I together with the state-of-the-art TIAs using a similar technology [7]–[10]. As can be seen, the proposed TIA with a cascaded CS configuration and PIP technique presents the highest Z_T and GBW$/P_{DC}$ among the published TIAs. On the other hand, sensitivity of the proposed TIA is slightly lower than those in [9] and [10]. The TIA presented in [9] used the feedback topology. A low sensitivity is relatively easier to achieve, whereas the GBW product is generally smaller. Note that the sensitivity of [10] may be significantly reduced if an input capacitance C_{pd} (450 fF in this case) was considered, which can lower the input impedance resulting in an increased input-referred noise current.

IV. Conclusion

With the proposed GBW enhancement technique of PIP and the optimized stage number considering the tradeoff between gain and power consumption, a 10-Gb/s TIA with a Z_T of 75 dB $\cdot\ \Omega$ and a GBW$/P_{DC}$ of 441.1 GHz $\cdot\ \Omega/$mW was realized in a 0.18-μm CMOS technology. The high Z_T and sufficient output voltage swing make the proposed TIA to be easily integrated with the post-stage mixed-mode and digital circuit blocks in an optical receiver chain.

References

[1] Z. Lao *et al.*, "20-Gb/s 14-kΩ transimpedance long-wavelength MSM-HEMT photoreceiver OEIC," *IEEE Photon. Technol. Lett.*, vol. 10, no. 5, pp. 710–712, May 1998.

[2] S. M. Park and H.-J. Yoo, "1.25-Gb/s regulated cascade CMOS transimpedance amplifier for gigabit ethernet applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 112–121, Jan. 2004.

[3] S. M. Park, J. Lee, and H.-J. Yoo, "1-Gb/s 80-dBΩ fully differential CMOS transimpedance amplifier in multichip on oxide technology for optical interconnects," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 971–974, Jun. 2004.

[4] A. A. Abidi, "On the choice of optimum FET size in wide-band transimpedance amplifiers," *J. Lightw. Technol.*, vol. 6, no. 1, pp. 64–66, Jan. 1988.

[5] C. Toumazou and S. M. Park, "Wideband low noise CMOS transimpedance amplifier for gigahertz operation," *Electron. Lett.*, vol. 32, no. 13, pp. 1194–1196, Jun. 1996.

[6] S. M. Park and S. Hong, "A 65-mW 5-Gb/s/ch current-mode common-base transimpedance amplifier array for optical interconnects," *IEEE Photon. Technol. Lett.*, vol. 15, no. 8, pp. 1138–1140, Aug. 2003.

[7] A. K. Petersen, K. Kiziloglu, T. Yoon, F. Williams, Jr, and M. R. Sandor, "Front-end CMOS chipset for 10 Gb/s communication," in *Dig. Symp. RFIC*, Jun. 2003, pp. 93–96.

[8] C. -H. Wu, C. -H. Lee, W. -S. Chen, and S. -I. Liu, "CMOS wideband amplifiers using multiple inductive-series peaking technique," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 548–552, Feb. 2005.

[9] B. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1263–1270, Aug. 2004.

[10] H.-Y. Hwang, J.-C. Chien, T.-Y. Chen, and L.-H. Lu, "A CMOS tunable transimpedance amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 12, pp. 693–695, Dec. 2006.

[11] J.-D. Jin and S. S. H. Hsu, "40-Gb/s transimpedance amplifier in 0.18-μm CMOS technology," *ESSCIRC*, pp. 520–523, Sep. 2006.

[12] J.-D. Jin and S. S. H. Hsu, "A 40-Gb/s transimpedance amplifier in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1449–1457, Jun. 2008.

[13] B. Razavi, *Design of Integrated Circuits for Optical Communications*. Singapore: McGraw-Hill, 2003.