A Miniaturized 70-GHz Broadband Amplifier in 0.13-μm CMOS Technology

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***Abstract*—A 70-GHz broadband amplifier is realized in a 0.13-μm CMOS technology. By using five cascaded common-source stages with the proposed asymmetric transformer peaking technique, the measured bandwidth and gain can reach 70.6 GHz and 10.3 dB under a power consumption ($P_{\rm DC}$) of 79.5 mW. Within the circuit bandwidth, the maximum input and output reflection coefficients are -6.1 and -10.8 dB, respectively. The group delay variation is $\pm$ 12.0 ps, and the output 1-dB compression point is 0.2 dBm at 5 GHz. With the miniaturized transformer design, the occupied core area of the circuit is only $\sim$ 0.05 mm^2. This amplifier demonstrates a gain-bandwidth product of 231 GHz and a GBW$/P_{\rm DC}$ up to 2.9 GHz/mW.**

***Index Terms*—Broadband amplifier, CMOS, common-source (CS) stage, gain-bandwidth product (GBW), transformer peaking.**

I. Introduction

THE millimeter-wave broadband amplifier is one of the key circuit blocks for high-speed optical communication systems. For wideband applications, previously reported results were mostly fabricated in III–V [1]–[3] or SiGe [4], [5] technologies to take advantage of the superior transistor characteristics. Lately, CMOS technology has also become an excellent candidate for wideband monolithic microwave integrated circuit (MMIC) amplifiers owing to the continuous scaling of device feature sizes. Recent advances successfully demonstrated several wideband amplifiers using CMOS technologies [6]–[17]. A recorded circuit bandwidth of 80 GHz was achieved by using a 90-nm CMOS technology [7].

For the amplifiers designed by MOSFETs, the circuit bandwidth is ultimately limited by the intrinsic capacitances (gate-source capacitance C_{gs}, gate–drain capacitance C_{gd}, and drain–source capacitance C_{ds}) of the transistors. Two design approaches are commonly adopted to alleviate the limitation for bandwidth extension in practical design, namely, the distributed amplifier (DA) topology [1]–[3], [6]–[11] and the inductive peaking techniques [12]–[17]. Fig. 1(a) shows the simplified circuit scheme for a MOS distributed amplifier. The termination resistors R_{MG} and R_{MD} are placed to minimize the destructive reflection for stability and gain flatness. With the intentional inductors (L_g and L_d), the input and output artificial transmission lines can be constructed by incorporating the equivalent gate and drain capacitances C_g and C_d, respectively. With a proper design of the transmission line delay, the output signal from each stage sums in phase, and makes it possible for a gain-bandwidth product (GBW) greater than that of an individual amplifier. However, to provide enough gain, the DA architecture normally consumes a large dc power and occupies a considerable amount of chip area. Fig. 1(b) shows a simple example of the inductive peaking topology, which is a common-source (CS) amplifier with shunt peaking [12]. Using a peaking inductor L_d connected in series with the load resistor R_d, the capacitive parasitics can be resonated out at the frequency around the original pole to extend the circuit bandwidth. The inductive peaking technique can achieve a large bandwidth under a small power consumption, while the overall circuit area is still limited by the size of the relatively large inductive components.

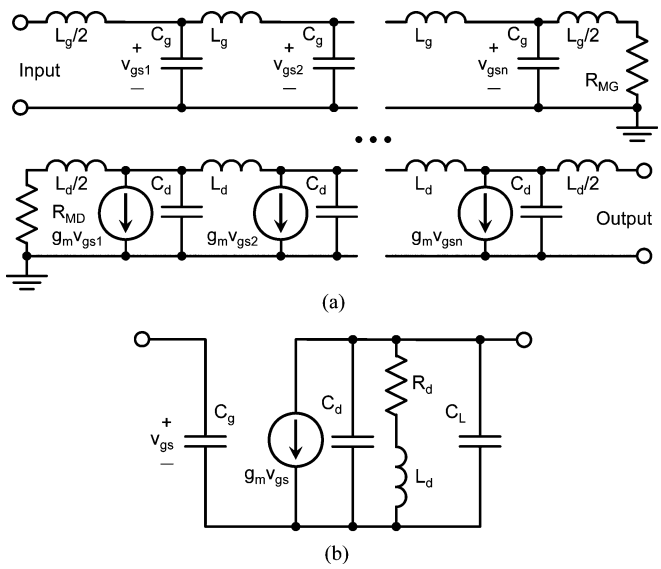

Fig. 1. (a) Simplified schematic representation of a MOS distributed amplifier. (b) CS stage with shunt peaking, where C_L is the effective loading capacitor.

In this study, a 0.13-μm CMOS broadband amplifier is realized using the proposed asymmetric transformer peaking technique in a cascaded CS configuration. By an effective frequency peaking design using transformers, this work achieves a bandwidth of 70.6 GHz under a low power consumption of 79.5 mW. With the miniaturized transformers utilizing the interconnect

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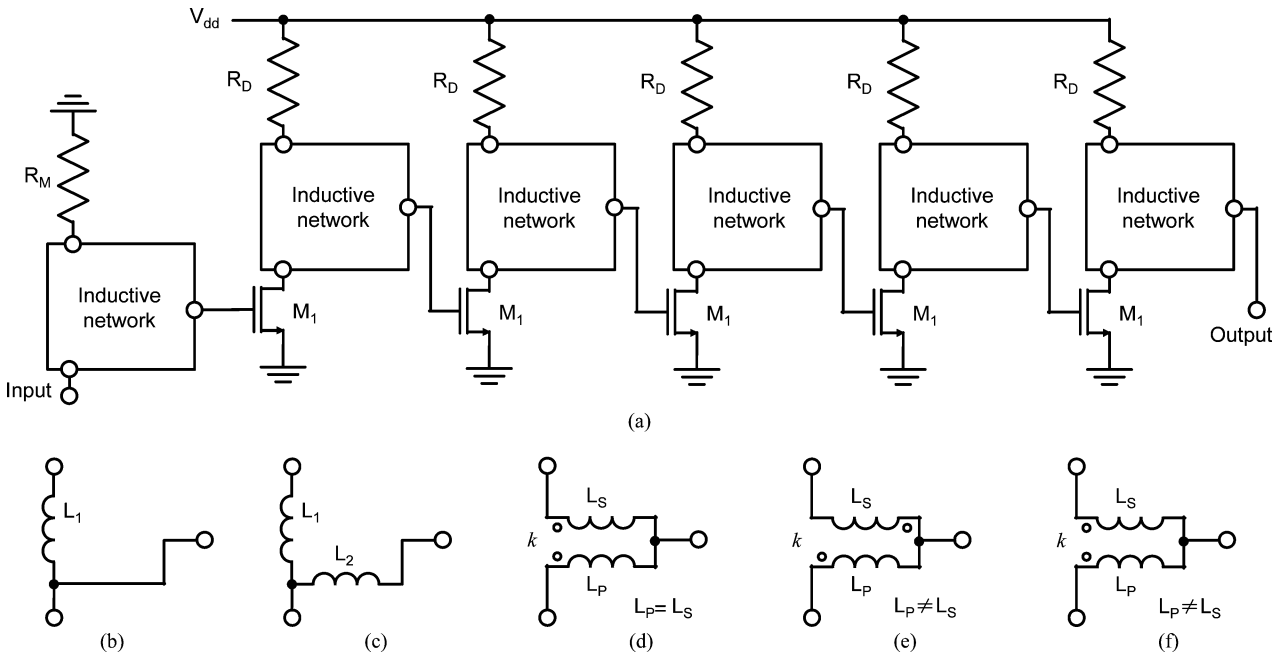

Fig. 2. (a) Basic amplifier configuration used in this study and comparison with different inductive peaking techniques. (b) Shunt peaking (c) Shunt-series peaking. (d) Symmetric transformer peaking. (e) Asymmetric T-coil peaking. (f) Asymmetric transformer peaking.

layers in CMOS process, the overall circuit core area is only ~ 0.05 mm^2.

This paper is organized as follows. Section II compares the effectiveness of different inductive peaking techniques based on the proposed amplifier topology. Section III presents the miniaturized transformer design and layout consideration in detail. The measured results are shown in Sections IV and V concludes this work.

II. Design of Broadband Amplifier

For low voltage and low power operation, the simple CS design is adopted in this study instead of the typically used cascode topology for high-frequency applications. As shown in Fig. 2(a), five CS stages are cascaded to provide a high gain amplification while still maintaining an overall low power consumption owning to the low supply voltage. Identical transistor size is employed to simplify the layout, where the gate width per finger is 5 μm and the finger number is eight. Note that the device size is optimized to achieve a large circuit bandwidth. A shunt resistor R_M is placed at the input for impedance matching. The drain resistor R_D in each stage functions as the load and also for the matching purpose. Further analysis of using different inductive peaking techniques will be illustrated as follows using the identical basic configuration of a five-stage CS design. Based on the foundry provided BSIM model and the ideal inductive components, these designs present a similar low-frequency gain but with an obvious bandwidth difference, as shown in Fig. 3.

A. Without Any Peaking Technique

Without applying any peaking technique, the three ports of the inductive network in each stage as shown in Fig. 2(a) are shorted to each other directly. Under a supply voltage of 1.5 V,

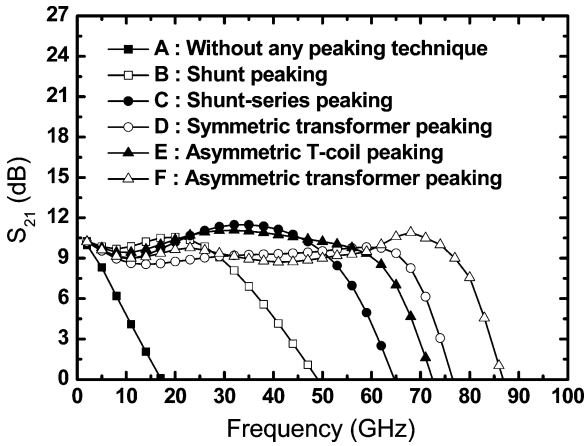

Fig. 3. Simulated frequency responses with different inductive peaking techniques.

the simulated low-frequency gain and bandwidth are 10.3 dB and 7.0 GHz, respectively, as shown in Fig. 3, curve *A*. The reason for such a small bandwidth is mainly due to the multiple *RC* poles in the circuit, and each of these results in a 20 dB/dec roll-off.

B. Shunt Peaking

The most straightforward bandwidth enhancement technique is probably shunt peaking [12]. As shown in Fig. 2(a) and (b), by placing an inductor in series with the resistor, C_d and C_g of the next stage can be canceled out by a shunt *LC* resonance. A different explanation is that the peaking inductor introduces an extra zero to extend the circuit bandwidth. By using an L_1 of 0.17 nH, the bandwidth is increased up to 34.1 GHz, as shown in Fig. 3, curve *B*.

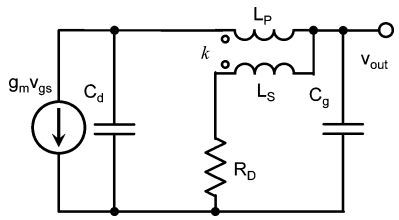

Fig. 4. Small-signal equivalent circuit model for one gain stage using symmetric transformer peaking technique.

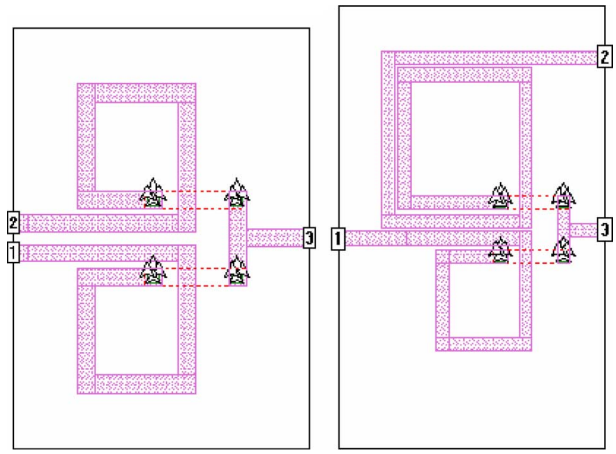

Fig. 5. On-chip transformer layouts for: (a) symmetric transformer T_M for input node and (b) asymmetric transformer T_D for the rest of the stages. The occupied areas are $53 \times 71\ \mu\text{m}^2$ and $63 \times 100\ \mu\text{m}^2$ for T_M and T_D, respectively.

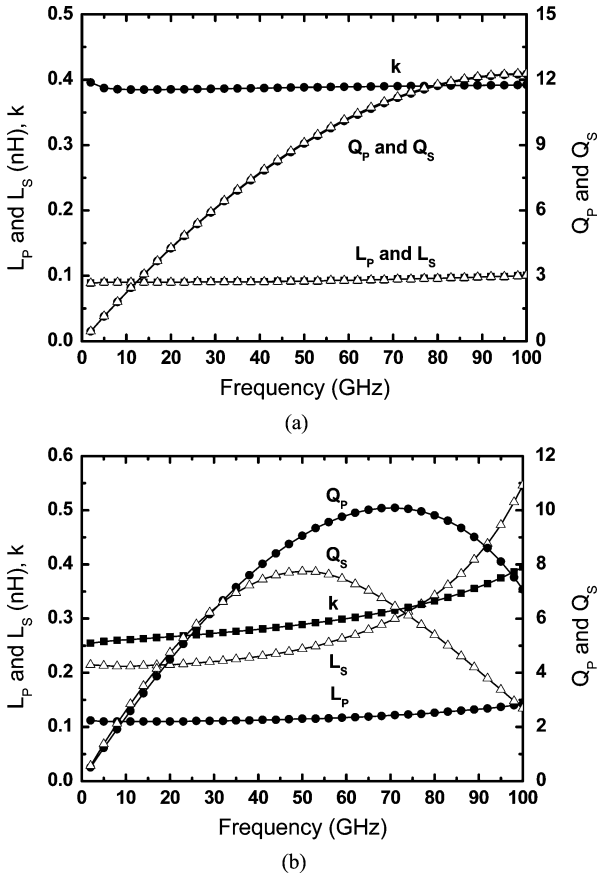

Fig. 6. Simulated frequency responses for: (a) T_M and (b) T_D.

C. Shunt-Series Peaking

For curve C, one more inductor is connected in series between the drain and the gate of the next stage to form the shunt-series peaking [13] as indicated in Fig. 2(c). These two inductors introduce one zero and two pairs of complex poles in the transfer function. Note that if the complex poles have a damping factor ξ smaller than $1/\sqrt{2}$, a gain peaking characteristics at around the corner frequency can be expected. In addition to the zero for bandwidth enhancement, one pair of the poles also shows a ξ value smaller than $1/\sqrt{2}$ for further gain peaking in this case. As a result, the bandwidth can be enhanced up to 55.5 GHz by using an L_1 of 0.11 nH and an L_2 of 0.09 nH.

D. Symmetric Transformer Peaking

As shown in Fig. 2(d), the symmetric transformer peaking technique has been reported for bandwidth enhancement [14], which has a positive coupling coefficient k and the identical primary coil L_P and secondary coil L_S inductances in the transformer. Based on the small-signal circuit model of one gain stage as shown in Fig. 4 (C_g is the gate capacitance of the next stage), the transimpedance transfer function $Z_T(s)$ from the current source $g_m v_{gs}$ to the node voltage v_{out} can be derived as (1), shown at the bottom of the following page. As can be observed from (1), one zero and two pairs of complex poles are also introduced, and both ξ values of the poles could be smaller than $1/\sqrt{2}$ if the circuit is properly designed. The simulated result presents an enhanced bandwidth up to 69.7 GHz with optimized $L_P = L_S = 0.11$ nH and $k = 0.1$, as shown in Fig. 3, curve D. However, the identical L_P and L_S used in this design may not be the optimal case due to the inherently unequaled loading capacitances from each side of the transformer.

E. Asymmetric T-Coil Peaking

As shown in Fig. 2(e), a recently published peaking technique, asymmetric T-coil peaking with a different L_P and L_S[15], is also presented for comparison. With the optimized $L_P = 0.12$ nH, $L_S = 0.08$ nH, and $k = 0.2$, the obtained bandwidth of the amplifier with asymmetric T-coil peaking is 64.7 GHz, as shown in Fig. 3, curve E. With a similar configuration but different transformer polarity, the derived Z_T from (1) can be applied here directly except that all the signs need to be inversed for the k-related terms. In other words, the coupling coefficient k here can be treated as negative if using the original equation. Compared with the transformer function in case D, this difference reduces the frequencies of the zero and the complex poles obtained from (1). Overall, the asymmetric transformer accommodates the unequaled parasitic loading capacitances in this design, while the inappropriate transformer polarity handicaps the effectiveness of bandwidth extension. As can be seen, these two factors somewhat compensate each other and the result is similar to that of curve D.

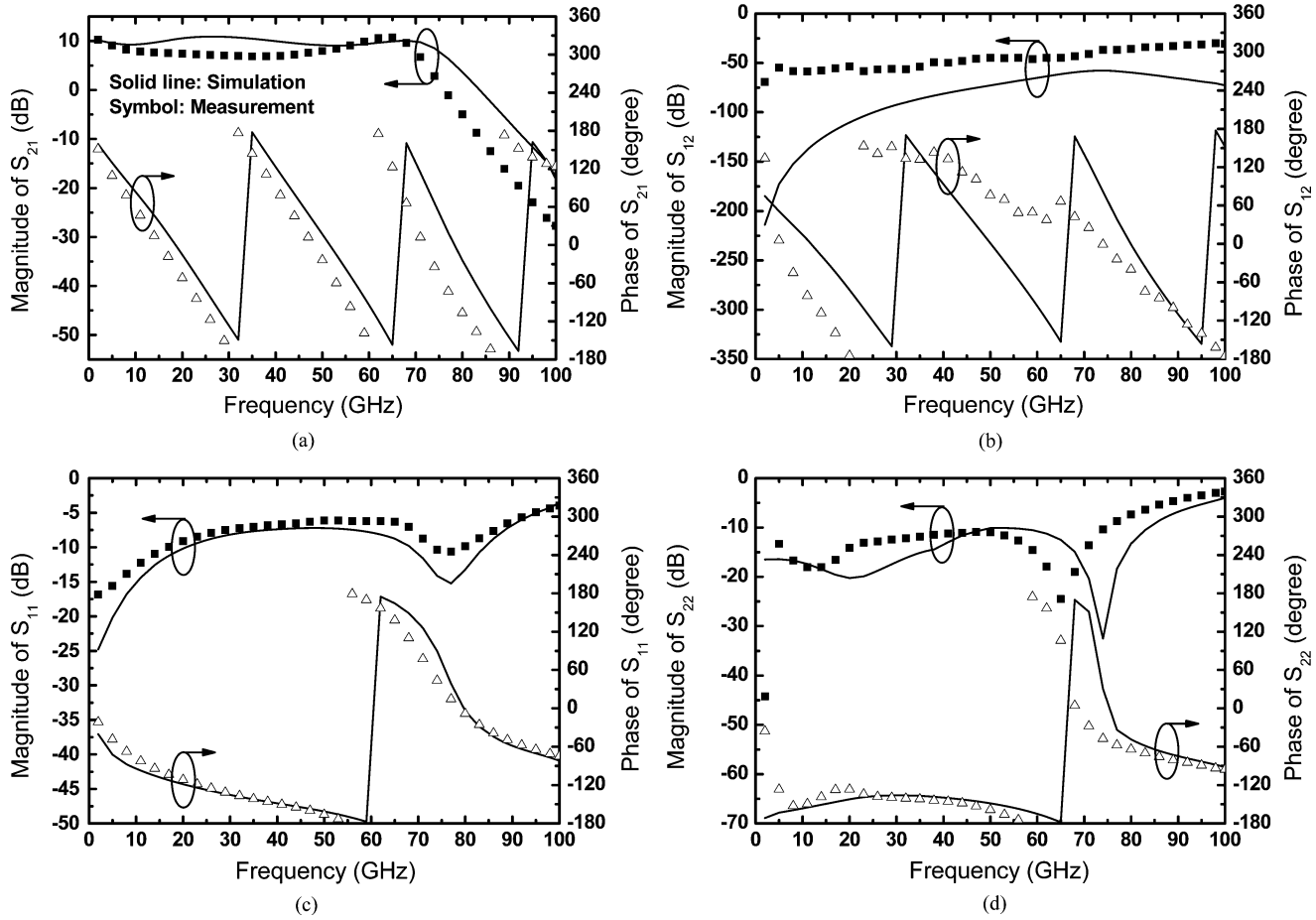

Fig. 7. Measured and simulated S-parameters of the proposed broadband amplifier using asymmetric transformer peaking.

F. Asymmetric Transformer Peaking

Based on the above analysis, the unequal inductances (case E with $L_P \neq L_S$) and an appropriate transformer polarity (case D with a positive k) are both beneficial to bandwidth enhancement. Here we propose the asymmetric transformer peaking configuration [16], as shown in Fig. 2(f). Similar to the transfer function (1), one zero and two pairs of complex conjugate poles are also introduced. By using the asymmetric transformer T_D, the circuit bandwidth can be enhanced up to 80.6 GHz with a gain flatness of ± 1.1 dB by $L_P = 0.11$ nH, $L_S = 0.2$ nH, and $k = 0.3$, as shown in Fig. 3, curve F. In our final design, the input transformer T_D is modified to be a symmetric one T_M for a better wideband input matching. As a result, the circuit bandwidth is further increased to 81.4 GHz (increased by $\sim 11.6\times$) with a better gain flatness of ± 1.0 dB . For the transformer T_M, the designed values are $L_P = L_S = 0.08$ nH and $k = 0.4$.

III. Transformer Design

For millimeter-wave design, layout plays a critical role for circuit performance. In this study, the transformer layout is co-designed with the active transistors for miniaturizing the geometry and reducing the loss from interconnect parasitics. In the adopted standard 0.13-μm CMOS process, one-poly and eight-metal layers (1P8M) with various thicknesses and spacings are available for the transformer design. For a high-Q on-chip transformer, the commonly used metal layer would be the top layer M8 owing to the thicker metal for a lower conductor loss. However, if considering the interconnects with

$$Z_T(s) = \frac{v_{\text{out}}}{-g_m v_{gs}} = R\frac{1 + s\dfrac{\left(L_S - k\sqrt{L_P L_S}\right)}{R}}{1 + sR\left(C_d + C_g\right) + s^2\left(L_P C_d + L_S C_d + L_S C_g\right) + s^2\left(-2k\sqrt{L_P L_S}C_d\right) + s^3 R L_P C_d C_g + s^4 L_P L_S C_d C_g\left(1-k\right)} \quad (1)$$

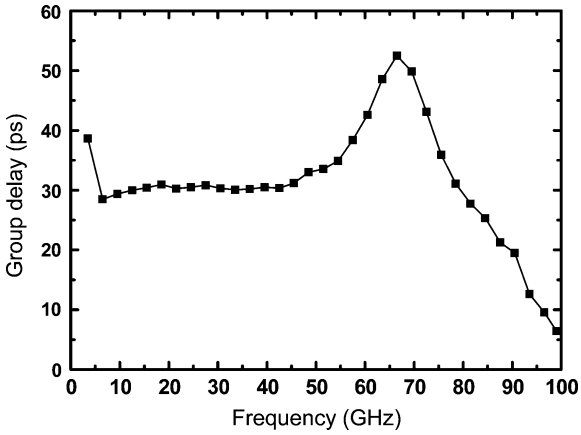

Fig. 8. Measured group delay of the proposed broadband amplifier.

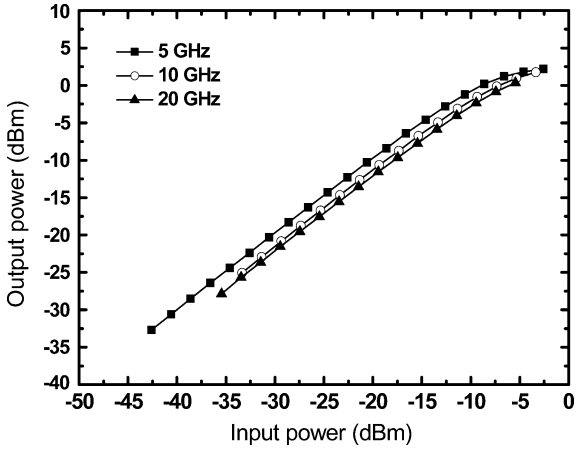

Fig. 9. Measured output power as a function of input power of the proposed broadband amplifier at three different frequencies.

the MOSFETs and the allowed minimum metal spacing, M8 may not be the best choice here.

In this design, M3 and M4 are finally selected for the layers of transformer winding and crossover. From the foundry provided process design kit (PDK), the RF layout of the transistors is based on a specific multi-finger configuration with the gate, drain, and source already connected to the M3 layer. Therefore, the transistors can be connected to the transformers directly by choosing the M3 layer. Compared with using the M8 layer for transformers, the additional loss introduced by the metal/via connections from M3 to M8 can be eliminated, which can be significant at the frequency of interest. In addition, the minimum metal spacing of M8 is restricted to 2 μm, while the M3 layer provides a spacing of 0.21 μm enabling a transformer with a higher coupling coefficient. For achieving the desired inductance ratio while maintaining design simplicity, two individually wound inductors are closely placed to form a transformer, as shown in Fig. 5(a) and (b). For the symmetric transformer T_M, the inner diameter is minimized to 15 μm for a small occupied area of $53 \times 71 \mu\text{m}^2$. For the asymmetric transformer T_D, the inner diameters of L_P and L_S are 17 and 26 μm, respectively, with a total area of $63 \times 100\ \mu\text{m}^2$. By using the EM simulator SONNET [18], the simulated results for T_M presents a Q of 11.2, an inductance of 0.095 nH, and a k of 0.39 at 70 GHz, as shown in Fig. 6(a). For transformer T_D, the Q of L_P is 10.1, that of L_S is 6.5, L_P is 0.122 nH, L_S is 0.3 nH, and k is 0.32 at 70 GHz, as shown in Fig. 6(b). By carefully considering the transformers and the active transistors simultaneously, the total interconnect lengths in the whole circuit are less than 50 μm.

IV. Measurement Results

The broadband amplifier was fabricated in a standard 1P8M 0.13-μm CMOS process. The ground-signal-ground (GSG) RF probes were used for the on-wafer S-parameters measurement from 2 to 100 GHz, as shown in Fig. 7 together with the simulated results. Note that the simulated results shown here consider the actual passive components using the EM tool. Compared with curve F in Fig. 3, the bandwidth reduces by about 7 GHz. The measured S_{21} at low frequencies is 10.3 dB and the circuit bandwidth is 70.6 GHz under a power consumption

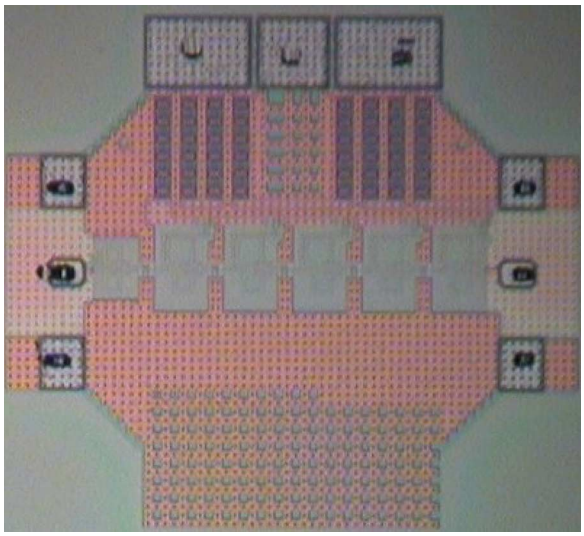

Fig. 10. Chip photograph (Chip area: $0.66 \times 0.59\text{mm}^2$, core area: $0.48 \times 0.11\text{mm}^2$).

P_{DC} of 79.5 mW. A GBW of 231 GHz and a GBW/P_{DC} of 2.9 GHz/mW are achieved. The measured reverse isolation S_{12} is well below -30 dB up to 100 GHz. In addition, the measured S_{11} and S_{22} are below -6.1 and -10.8 dB, respectively, within the circuit bandwidth. Compared with the simulated S_{21}, the low-frequency gain is similar but the circuit bandwidth is dropped by about 4 GHz. A difference between the measured and simulated phase of S_{21} is also observed especially at high frequencies. Moreover, an obvious difference can be seen for S_{12} in both magnitude and phase. These discrepancies may be due to the limited accuracy of the transistor model which is verified only to 30 GHz. In addition, although the passive components such as transformers and the interconnects were carefully simulated by the EM tool, the coupling effect among the various passive/active components and the substrate is not included in the simulation. Fig. 8 shows the group delay as a function of frequency. Within the circuit bandwidth, the group delay is in a range of 28.5 to 52.5 ps. A group delay ripple GD_{pp} of $\pm$ 12.0 ps is obtained.

TABLE I
SUMMARY OF THE STATE-OF-THE-ART CMOS BROADBAND AMPLIFIERS

Ref.	This work	[6]	[7]	[8]	[9]	[10]	[11]
BW (GHz)	70.6	43.9	80	70	50	45.6	39.4
Gain (dB)	10.3	10	7.4	7	9.5	6.7	20
GBW (GHz)	231	139	190	157	150	99	394
S_{11} (dB)	-6.1	-14	-8	-7	-10	-10	-10
S_{22} (dB)	-10.8	-8	-10	-12	-12	-10	-10
GD_{pp} (ps)	24	—	—	20	10	—	16
$P_{1dB,out}$ (dBm)	0.2	—	8	11	7	—	6.5
Chip area (mm^2)	0.39	1.50	0.72	0.72	1.54	1.89	2.24
Core area (mm^2)	0.05	~ 1.10	~ 0.44	~ 0.48	~ 1.05	~ 1.36	~1.95
Voltage (V)	1.5	—	2.4	—	—	3.3	2.8
Power (mW)	79.5	103	120	122	420	497	250
GBW/P_{DC} (GHz/mW)	2.9	1.3	1.6	1.3	0.4	0.2	1.6
CMOS Technology	0.13-μm	0.13-μm	90-nm	90-nm	0.18-μm	0.18-μm	0.18-μm

Fig. 9 shows the results of the output power versus the input power at three different frequencies to investigate the circuit linearity. The measured output 1-dB compression points $P_{1\ \mathrm{dB}\mathrm{out}}$ are 0.2, -0.2, and -1.0 dBm at 5, 10, and 20 GHz, respectively. The chip area including the dc and RF probing pads is 0.66×0.59 mm^2, while the core area is only 0.48×0.11 mm^2 (~ 0.05 mm^2), as shown in Fig. 10.

The circuit performances are summarized in Table I together with the published state-of-the-art CMOS broadband amplifiers [6]–[11]. Compared with these amplifiers, this work achieves the highest $\mathrm{GBW}/P_{\mathrm{DC}}$ of 2.9 GHz/mW and the lowest power consumption of 79.5 mW. In addition, the core area is only ~ 0.05 mm^2, which is the smallest one among the works listed in this table.

V. CONCLUSION

A 10-dB 70-GHz broadband amplifier was successfully demonstrated in a standard 0.13-μm CMOS technology. By using the proposed asymmetric transformer peaking technique together with a simple CS cascaded design, the amplifier achieved the highest $\mathrm{GBW}/P_{\mathrm{DC}}$ figure-of-merits among the published CMOS broadband amplifiers. In addition, the core circuit of this design only occupied a chip area of ~ 0.05 mm^2.

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