A 40-Gb/s Transimpedance Amplifier in 0.18-μm CMOS Technology

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***Abstract*—A 40-Gb/s transimpedance amplifier (TIA) is realized in 0.18-μm CMOS technology. From the measured S-parameters, a transimpedance gain of 51 dBΩ and a 3-dB bandwidth up to 30.5 GHz were observed. A bandwidth enhancement technique, π-type inductor peaking (PIP), is proposed to achieve a bandwidth enhancement ratio (BWER) of 3.31. In addition, the PIP topology used at the input stage decreases the noise current as the operation frequency increases. Under a 1.8 V supply voltage, the TIA consumes 60.1 mW with a chip area of 1.17 $\times$ 0.46 mm^2. The proposed CMOS TIA presents a gain–bandwidth product per DC power figure of merit $(\mathrm{GBP}/P_{\mathrm{dc}})$ of 180.1 GHzΩ/mW.**

***Index Terms*—Bandwidth enhancement technique, CMOS, gain–bandwidth product, transimpedance amplifier (TIA), π-type inductor peaking.**

I. Introduction

THE rapidly increased demands for large data capacity has pushed the data rate of optical communication systems from 10 Gb/s (OC-192) up to 40 Gb/s (OC-768) [1]–[9]. For optoelectronic integrated circuits (OEICs) with such a high operation speed, the design for low cost, low power consumption, and high integration level becomes a real challenge. Considering the above requirements, the CMOS-based technology is probably the best candidate, while the capability of wideband operation can be seriously limited by the inherent capacitances in a MOS transistor.

A simple approach to improve the circuit bandwidth is shunt peaking [10], which introduces an inductor to resonate with the inherent capacitances and gives a bandwidth enhancement ratio (BWER) of 1.85 for a cascaded common-source (CS) stage. Two inductive peaking techniques, T-coil peaking [11] and shunt-series peaking [4], with BWERs of 2.82 and 3.46 were also proposed. However, the BWERs were calculated under certain assumptions, which may not be practical in real circuits. For example, the drain capacitances were neglected for T-coil peaking and the ratio of the gate to drain capacitances was set to be one for shunt-series peaking. Discrepancies between the real circuits and the assumptions may degrade the expected bandwidth.

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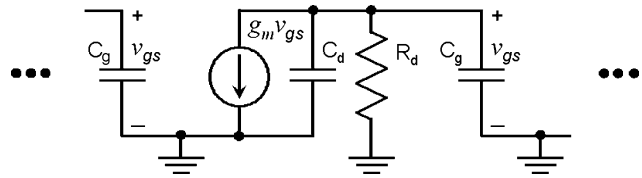

Fig. 1. Small-signal equivalent circuit model of a cascaded common-source amplifier.

In this paper, an effective wideband technique, the π-type inductor peaking (PIP), is proposed to further improve the bandwidth by resonating with the intrinsic capacitances of the devices [5]. Composed of three inductors, PIP can significantly enhance the bandwidth of a cascaded CS stage by a BWER of 3.31. A transimpedance amplifier (TIA) is realized in a 0.18-μm CMOS technology to demonstrate this design approach. In addition to the bandwidth enhancement, TIA designed with PIP presents a trend of decreasing input-referred noise current as the operation frequency increases in the desired bandwidth. Moreover, the grounded coplanar-waveguide (GCPW) structure is employed for interconnects in this design to provide a better signal shielding and reduce loss at high frequencies [12], [13].

This paper is organized as follows. A comparison between three inductive peaking approaches published previously is presented in Section II. Section III describes the design concepts of the proposed PIP technique in a cascaded CS stage. The design tradeoffs are also discussed. A CMOS TIA using four cascaded CS stages with PIP configuration is presented in Section IV. A detailed noise analysis is presented in Section V. The measured results are shown in Section VI, and Section VII concludes this work.

II. Comparison of Different Wideband Techniques

For the small-signal equivalent circuit model of a cascaded CS amplifier, as shown in Fig. 1, we can assume that the 3-dB bandwidth of each stage is determined by the drain resistance R_d, equivalent drain capacitance C_d, and equivalent gate capacitance C_g of the next stage. The ratio of C_g to C_d can be determined from the BSIM 3 model provided by the foundry for a more practical estimation. The extracted C_g/C_d is frequency dependent, varying between 2.5 and 3.5 (0.5–60 GHz). To simplify the circuit analysis, C_g/C_d is set to be 3 here. Based on this small-signal circuit model, three different inductor peaking techniques are compared as follows.

As shown in Fig. 2, curve a shows the normalized frequency response of this circuit without any bandwidth enhancement method applied. With one inductor connected in series with R_d, the maximum achievable BWER is 1.85 with a gain peaking of

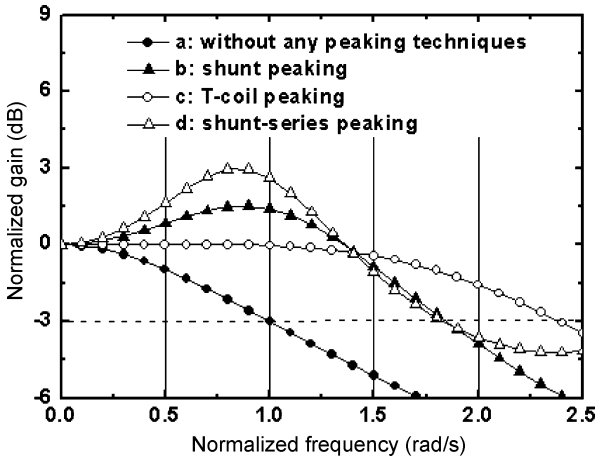

Fig. 2. Bandwidth improvement by three previously published wideband techniques.

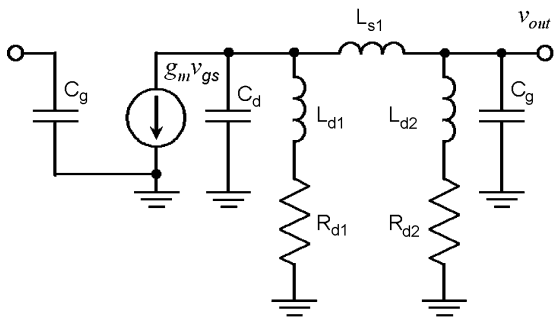

Fig. 3. The equivalent circuit model of one gain stage with the π-type inductor peaking (PIP) technique.

1.5 dB, as shown in Fig. 2, curve b [10]. A more effective technique is the T-coil peaking which utilizes one transformer and one capacitor, and provides a BWER of 2.82 if C_d is neglected [11]. Note that the value obtained in Fig. 2, curve c is 2.40 since C_d is taken into account for a fair comparison. The third technique is shunt-series peaking [4] which employs two inductors, one is in series with R_d and the other is with C_g. The original circuit analysis presented in [4] shows a BWER of 3.46 with a gain peaking of 1.8 dB based on the assumption that the ratio of C_g to C_d is one. However, the value is reduced to 1.83 when a more practical ratio of three is used, as shown in Fig. 2, curve d. In this paper, a more effective bandwidth extension technique is proposed. On the basis of including the drain capacitance C_d, and with a C_g/C_d ratio of 3, an improved BWER up to 3.31 can be obtained. The details are discussed in the following sections.

III. π-Type Inductor Peaking

A. Design Concept of PIP

Fig. 3 shows the small-signal equivalent circuit model of a cascaded CS stage including the PIP inductors (L_{d1}, L_{s1}, and L_{d2}), where R_{d1} and R_{d2} are the drain bias resistors. The progressive bandwidth improvement by adding each peaking inductor is described as follows.

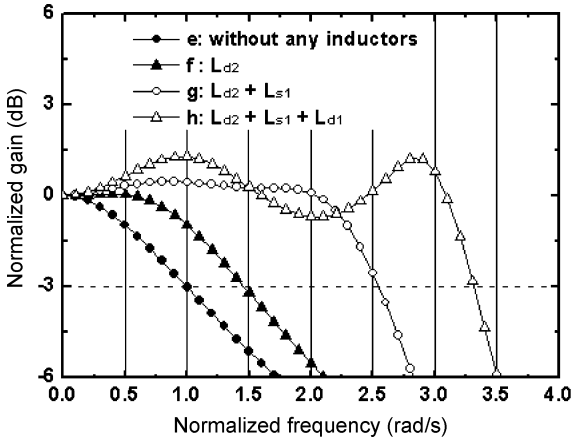

Fig. 4. Comparison of the bandwidth enhancement results using PIP technique under different numbers of peaking inductors, where $C_g = 3_{Cd}$ and $R_{d1} = R_{d2}$.

Without the PIP inductors, the drain current $g_m v_{gs}$ flows into C_d, C_g, R_{d1}, and R_{d2}, and generates the output voltage $v_{\rm out}$. In this case, the 3-dB bandwidth ω_0 is limited by the resistive and capacitive loads. By inserting L_{d2} in series with R_{d2}, the bandwidth is increased by a parallel resonance with C_d and C_g. An alternative explanation is that the inductor delays the transient current into R_{d2} and forces more current to flow into the loading capacitor, which improves the speed of the output transient signal and results in an increased circuit bandwidth. If L_{s1} is also employed, the bandwidth can be further enhanced by a series resonance with C_g at higher frequencies, which forces more drain current to flow through L_{s1} and reach the output terminal. In time domain, the transient current charges the two capacitors separated by L_{s1} at different times. As a result, the charging time is reduced leading to an improved bandwidth. Finally, by introducing one more inductor L_{d1}, C_d and C_g can be resonated in parallel with L_{d1} at even higher frequencies to obtain a further enhanced bandwidth. Based on the circuit shown in Fig. 3, Fig. 4 shows the frequency response of the above four conditions, where ω_0 and the DC gain are both normalized. The gradually improved bandwidth can be observed as adding the three peaking inductors step by step.

B. Transfer Function of PIP

To obtain a more comprehensive understanding of the frequency response, the transimpedance transfer function $Z_{\rm PIP}(s)$ of the circuit in Fig. 3 is derived as

$$Z_{\rm PIP}(s) = \frac{v_{\rm out}}{-g_m v_{gs}} = R_{d1}R_{d2}\frac{1+s\left(\frac{L_{d1}}{R_{d1}}+\frac{L_{d2}}{R_{d2}}\right)+s^2\frac{L_{d1}}{R_{d1}}\frac{L_{d2}}{R_{d2}}}{D_0+sD_1+s^2D_2+s^3D_3+s^4D_4+s^5D_5} \quad (1)$$

where

$$\begin{aligned} D_0 &= R_{d1}+R_{d2} \\ D_1 &= L_{d1}+L_{d2}+L_{s1}+R_{d1}R_{d2}(C_d+C_g) \\ D_2 &= (C_d+C_g)(R_{d1}L_{d2}+R_{d2}L_{d1}) \\ &\quad + R_{d1}L_{s1}C_d + R_{d2}L_{s1}C_g \end{aligned}$$

TABLE I
PROPERTIES OF THE POLES AND ZEROS OF ONE GAIN STAGE WITH PIP UNDER DIFFERENT NUMBERS OF PEAKING INDUCTORS

	without PIP	L_{d2}	$L_{d2}+L_{s1}$	$L_{d2}+L_{s1}+L_{d1}$
Zero	—	$\omega_{z1}=1.33$	$\omega_{z1}=1.33$	$\omega_{z1}=1.33$ $\omega_{z2}=2.50$
Pole	$\omega_{p1}=1.00$	—	—	$\omega_{Ld1,p3}=1.39$
Complex pole	—	$\omega_{Ld2,p1}=\omega_{Ld2,p2}$ $=1.15$	$\omega_{Ls1,p1}=\omega_{Ls1,p2}$ $=1.21$ $\omega_{Ls1,p3}=\omega_{Ls1,p4}$ $=2.37$	$\omega_{Ld1,p1}=\omega_{Ld1,p2}$ $=1.28$ $\omega_{Ld1,p4}=\omega_{Ld1,p5}$ $=3.01$
Damping factor	—	$\xi_{Ld2,p1}=0.79$	$\xi_{Ls1,p1}=0.82$ $\xi_{Ls1,p3}=0.28$	$\xi_{Ld1,p1}=0.63$ $\xi_{Ld1,p4}=0.14$

$$\begin{aligned} D_3 &= L_{d1}C_d(L_{d2}+L_{s1}) \\ &\quad + L_{d2}C_g(L_{d1}+L_{s1}) + R_{d1}R_{d2}L_{s1}C_dC_g \\ D_4 &= L_{s1}C_dC_g(R_{d1}L_{d2}+R_{d2}L_{d1}) \\ D_5 &= L_{d1}L_{d2}L_{s1}C_dC_g \end{aligned} \tag{2}$$

As can be clearly observed, two zeros (R_{d1}/L_{d1} and R_{d2}/L_{d2}) existed in $Z_{\rm PIP}(s)$. By an appropriate design, the zeros can be employed to enhance the bandwidth. The required inductances for bandwidth improvement are determined one by one analytically as follows.

To derive L_{d2}, the effects of L_{d1} and L_{s1} are first neglected by setting $L_{d1}=L_{s1}=0$ in (1). Normalized by the DC impedance $R_{d1}//R_{d2}$, the transfer function $z_{Ld2}(s)$ becomes

$$z_{Ld2}(s)=\frac{1+sL_{d2}/R_{d2}}{1+s\frac{(L_{d2}+R_{d1}R_{d2}(C_d+C_g))}{R_{d1}+R_{d2}}+s^2\frac{R_{d1}L_{d2}(C_d+C_g)}{R_{d1}+R_{d2}}}. \tag{3}$$

The equation indicates that the numerator includes a zero $\omega_{z1}=R_{d2}/L_{d2}$ and the denominator contains a pair of complex conjugate poles $\omega_{Ld2,p1}$ and $\omega_{Ld2,p2}$, which can be written as

$$\begin{aligned} &s^2+s\left(\frac{1}{R_{d1}(C_d+C_g)}+\frac{R_{d2}}{L_{d2}}\right)+\frac{R_{d1}+R_{d2}}{R_{d1}L_{d2}(C_d+C_g)} \\ &=(s+\omega_{Ld2,p1})\cdot(s+\omega_{Ld2,p2}) \\ &=s^2+s2\xi\omega_n+\omega_n^2 \end{aligned} \tag{4}$$

where ξ and ω_n are the damping factor and the corner frequency of the complex poles, respectively. Note that the frequency response can be affected by the value of ξ. For ξ smaller than $1/\sqrt{2}$, a gain-peaking characteristic can be observed at around ω_n. Therefore, the bandwidth can be enhanced not only by zero but also complex poles. Under $R_{d1}=R_{d2}$ and $C_g=3C_d$, the required inductance L_{d2} and the maximum achievable 3-dB bandwidth ω_{Ld2} can be derived from the equation $|z_{Ld2}(\omega_{Ld2})|^2=1/2$ with $\omega_0=1/(2R_{d1}C_d)$ [14]:

$$L_{d2}=m_{d2}\cdot R_{d1}^2\cdot C_d \tag{5}$$

where m_{d2} is 1.50, and the resulted ω_{Ld2} equals 1.46, as shown in Fig. 4, curve f. The improved bandwidth mainly results from the in-band ω_{z1} of 1.33, since the complex poles have a $\xi_{Ld2,p1}$ of 0.79 which is larger than $1/\sqrt{2}$. Based on (3)–(5), $\omega_{z1}=1/(1.5R_{d1}C_d)=1.33$, $\omega_{Ld2,p1}=\omega_{Ld2,p2}=\sqrt{1/(2L_{d2}C_d)}=1.15$, and $\xi_{Ld2,p1}=(1/(4R_{d1}C_d)+R_{d2}/L_{d2})/(2\omega_n)=0.79$. The properties of the poles and zeros as adding the three peaking inductors step by step are summarized in Table I.

After obtaining the required L_{d2}, the inductance L_{s1} can be derived from (1) by setting $L_{d1}=0$. The normalized transfer function $z_{Ls1}(s)$ includes additional complex poles of $\omega_{Ls1,p3}$ and $\omega_{Ls1,p4}$. To derive the required inductance and the maximum enhanced bandwidth ω_{Ls1}, (5) is used. A similar equation for L_{s1} can be obtained as

$$L_{s1}=m_{s1}\cdot R_{d1}^2\cdot C_d \tag{6}$$

where m_{s1} is 0.86, and the associated ω_{Ls1} equals 2.55 with a gain variation of 0.5 dB, as shown in Fig. 4, curve g. The bandwidth is improved mainly by both the in-band ω_{z1} of 1.33, and the additional complex poles with a $\xi_{Ls1,p3}$ of 0.28 and a $\omega_{Ls1,p3}$ ($\omega_{Ls1,p4}$) of 2.37. The above values are determined based on the denominator of $z_{Ls1}(s)$.

To derive the inductance L_{d1} for a maximum achievable bandwidth ω_{Ld1}, the previously obtained L_{d2} and L_{s1} are both taken into account. With the normalized (1) by the DC impedance $R_{d1}//R_{d2}$ and (5)–(6), the derived result is

$$L_{d1}=m_{d1}\cdot R_{d1}^2\cdot C_d \tag{7}$$

where m_{d1} is 0.80, and the resulted ω_{Ld1} equals 3.31 with a gain variation of 2.0 dB, as shown in Fig. 4 curve h. The first gain peaking at around ω_0 is due to the complex poles with a $\xi_{Ld1,p1}$ of 0.63 and the in-band zero ω_{z1} of 1.33, while the second peaking at around $3\omega_0$ results from the complex poles with a $\xi_{Ld1,p4}$ of 0.14 and the in-band zero ω_{z2} of 2.50. The zero ω_{z2} of 2.50 is calculated from R_{d1}/L_{d1}.

C. Design Tradeoffs in PIP Configuration

The above analysis illustrates the impact of each PIP inductor on the BWER and gain variation under the condition $R_{d1}=R_{d2}$ and $C_g=3C_d$. It is also of interest to investigate the circuit performance if using different values of m_{d2}, m_{s1}, m_{d1}, C_g/C_d, and R_{d1}/R_{d2}, which provides guidelines toward the optimal design and a deeper understanding of the PIP configuration.

Fig. 5 shows the impact of each PIP inductor on the frequency response under $R_{d1}=R_{d2}$ and $C_g=3C_d$. Under a fixed m_{s1}

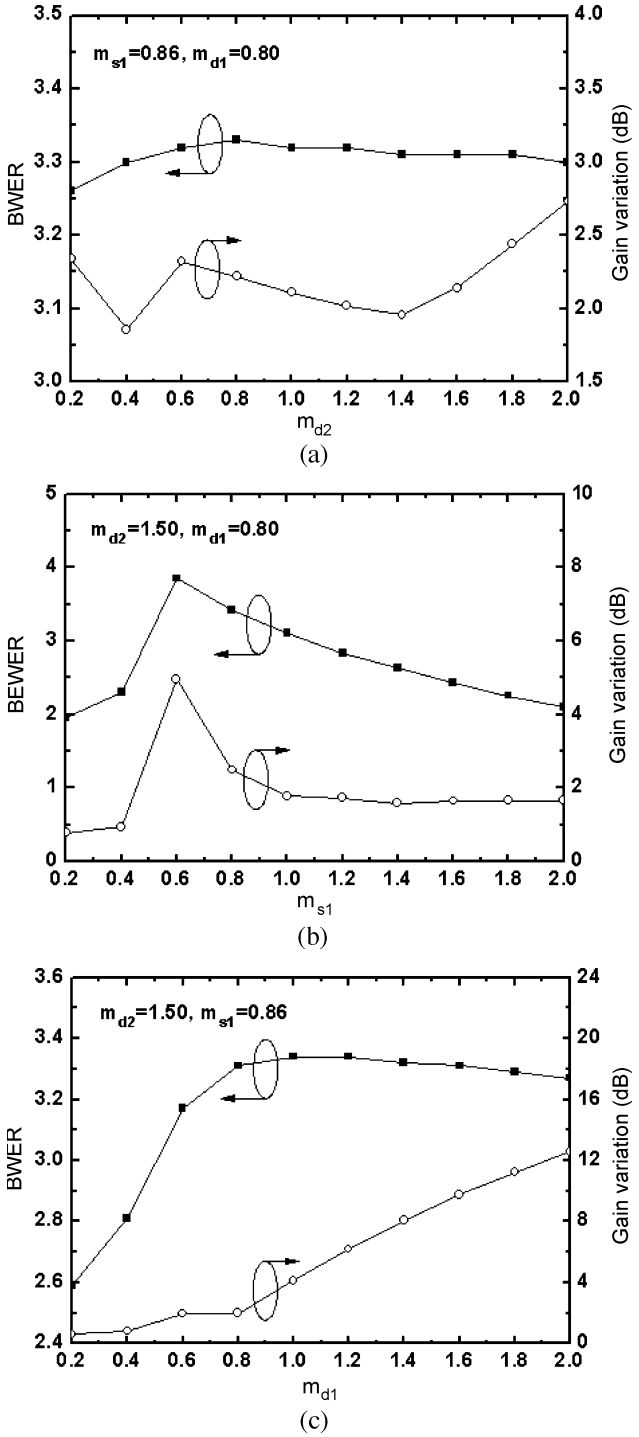

Fig. 5. The BWER and gain variation with different PIP inductors (a) m_{d2}, (b) m_{s1}, and (c) m_{d1}.

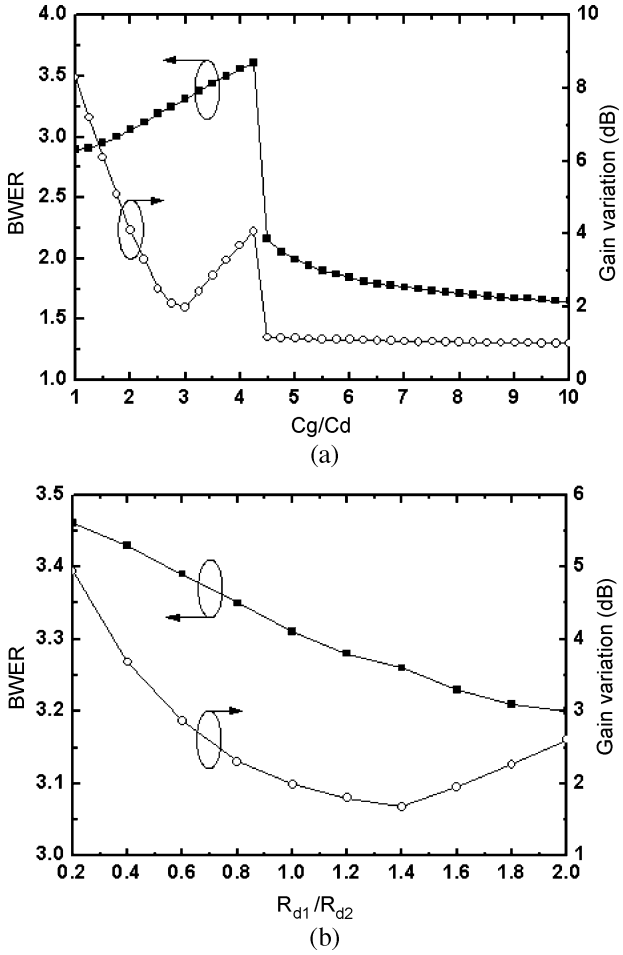

Fig. 6. The BWER and gain variation for different values of (a) C_g/C_d and (b) R_{d1}/R_{d2}.

of 0.86 and m_{d1} of 0.80, the BWER is not a strong function of m_{d2} in the range of 0.2–2.0, as shown in Fig. 5(a). The highest BWER of 3.33 can be obtained at $m_{d2} = 0.8$ with a gain variation of 2.2 dB. In Fig. 5(b), with an m_{s1} of 0.6, the BWER and the gain variation both reach the highest values of 3.85 and 5.0 dB, respectively. Although the bandwidth can be greatly improved, the signal distortion may be serious because of the large gain variation. In the range of 0.8–1.2, the gain variation is kept below 2.5 dB with a BWER larger than 2.84, which is more suitable for a practical design. The dependence of the BWER and gain variation on m_{d1} is illustrated in Fig. 5(c). For a lower gain variation while maintaining a high BWER, a better choice of m_{d1} should be around 0.8. Considering the tradeoffs between a large BWER and a small gain variation, the previously obtained values of $m_{d2} = 1.50$, $m_{s1} = 0.86$, and $m_{d1} = 0.80$ are very close to the optimal result.

Fig. 6 plots the BWER and gain variation as a function of C_g/C_d and R_{d1}/R_{d2}. In more general cases, C_g/C_d could vary from 1 to 10 for different circuit topologies or extra source/load capacitances [15]. Within the range of 2.5 to 3.5 of C_g/C_d, high BWER values in a range of $3.15 \sim 3.46$ can be achieved in a gain variation between 2.0 dB and 3.0 dB, as shown in Fig. 6(a). On the other hand, the BWER reduced monotonically as R_{d1}/R_{d2} increases as shown in Fig. 6(b). For a small R_{d1}/R_{d2} of 0.2, the BWER can be as high as 3.46 but with a gain variation up to 4.94 dB. The gain variation can be reduced to 1.68 dB with a smaller BWER of 3.26 by choosing a R_{d1}/R_{d2} of 1.4. The selected R_{d1}/R_{d2} of 1 in the final design is simple and around the optimal value for both BWER and gain flatness.

IV. 40-Gb/s TIA

To demonstrate the proposed PIP technique, a TIA targeting at 40 Gb/s is realized in 0.18-μm CMOS technology. The

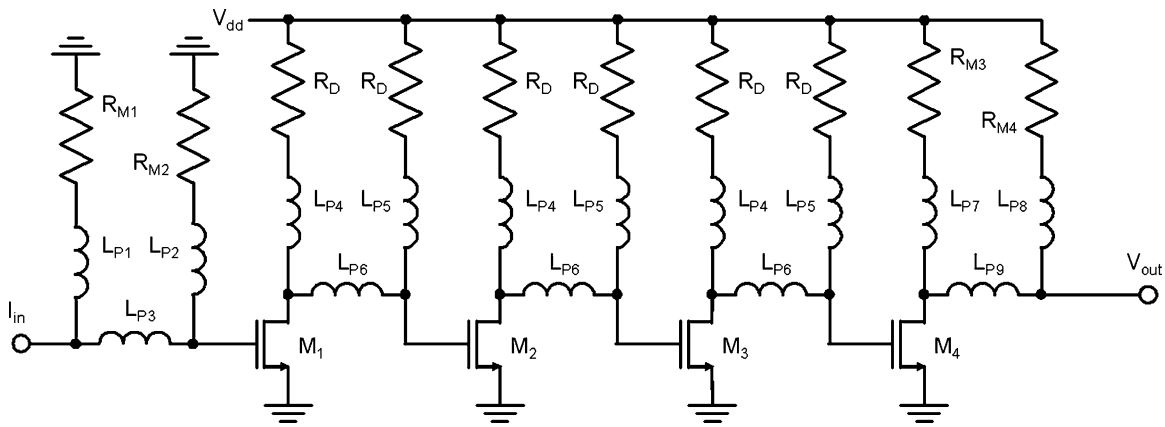

Fig. 7. Circuit topology of the proposed 40-Gb/s CMOS TIA with PIP.

40-Gb/s TIA composes of four cascaded CS stages, as shown in Fig. 7. For a cascaded amplifier with identical first-order gain stages, the optimal stage number $(n_{\rm opt})$ can be estimated by a simple equation of $2 \times \ln(A_{\rm tot})$ to achieve a maximized circuit bandwidth, where $A_{\rm tot}$ is the total voltage gain [16]. Note that $A_{\rm tot}$ is equivalent to the overall S_{21} under the matched input and output impedances of 50 Ω. For the proposed TIA with an $A_{\rm tot}$ of 16.7 dB, the finally designed stage number is 4. Identical resistance for the drain bias resistors (R_D) of each stage is employed, and the input and output impedances are designed as 50 Ω through the resistors R_{M1}–R_{M4}. Note that the 50-Ω input impedance is mainly for high-frequency measurement consideration, which may not be the optimal design if considering the electrical characteristics of the photodiode. For a high-gain characteristic, a large R_D is preferred. However, the required peaking inductances for PIP topology, as derived in Section III, are proportional to R_D^2. It can be seen that a tradeoff exists here since a large inductor not only occupies a large chip area but also causes difficulties to maintain an inductive characteristic up to the circuit bandwidth. In addition, the resistive parasitics of the inductors can degrade the circuit performance. This effect is more obvious for the series-connected inductors (L_{s1}) in PIP configuration. In practical design, these inductors are designed to be smaller than the calculated values to reduce the resistive loss. The optimized R_D obtained for reasonable inductances while still providing high gain is 200 Ω. The adopted device width of M_1–M_3 is 48 μm with a f_T of $\sim$60 GHz and a $f_{\rm max}$ of $\sim$90 GHz (estimated from the foundry provided transistor model), while a larger width of 64 μm is employed for M_4 to increase the gain and the output signal swing under a 50-Ω load. The inductances $(L_{P1}$–$L_{P9})$ are designed based on the derived (5)–(7), while some optimizations are essential due to the frequency dependence of C_g/C_d and the parasitic effects of the on-chip inductors. The finally designed values are $L_{P1} = 0.85$ nH, $L_{P2} = L_{P3} = 0.48$ nH, $L_{P4} = L_{P5} = L_{P7} = L_{P8} = 1.6$ nH, $L_{P6} = 0.42$ nH, and $L_{P9} = 0.2$ nH. Compared with the theoretical value, a smaller BWER of 2.88 (simulated) for the single-stage amplifier using PIP (one of the three identical stages in the final design, see Fig. 7) is obtained in actual implementation.

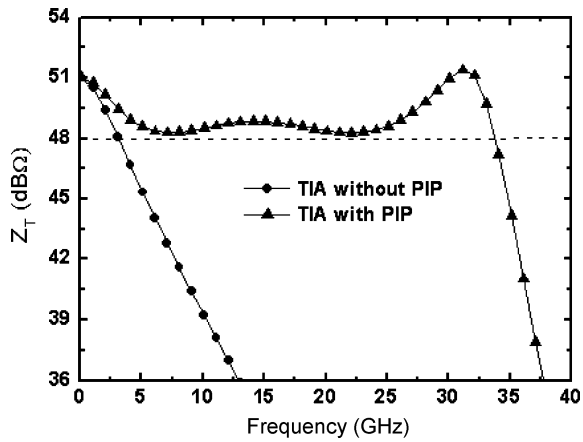

Fig. 8. Simulated frequency response for the TIA with and without PIP.

Fig. 8 compares the design of a TIA with and without using PIP technique. With a transimpedance gain Z_T of 51 dBΩ, the simulated bandwidth for the TIA with PIP is improved by a factor up to $\sim$11 (33.8 GHz/3.1 GHz) compared to that without PIP. It is worth to point out that a photodiode capacitance (C_{pd}) of 50 fF is incorporated at the TIA input monolithically by the MIM capacitor in CMOS process, which is also the main limitation for the TIA bandwidth. By employing the PIP configuration $(L_{P1}$–$L_{P3})$ at the input stage, the capacitive loading from C_{pd} can be effectively resonated to achieve a wide bandwidth.

Note that special care should be taken for the layout of the circuit. For high-frequency circuits, the commonly used interconnect structures are microstrip (MS) line and coplanar waveguide (CPW). However, these two structures can suffer either from severe signal crosstalk or significant signal loss from the lossy silicon substrate [17]. In this design, GCPW configuration is employed to prevent the above problems [12], [13]. The sidewall and bottom ground planes realized by various metal layers are utilized for a better shielding of the signal paths. The total length of the signal paths in the designed TIA is about 500 μm, which has an insertion loss of only 1.1 dB at 33.8 GHz estimated using an EM simulator [18]. In addition, the lines are all

designed as 50 Ω to alleviate the additional capacitive loading effect on the circuit.

V. Noise Analysis

The input-referred noise current $i_{n,in}$ is an important issue for TIA design, which determines the sensitivity of the circuit. For the cascaded configuration, the input-referred noise is dominated by the first stage, since the impact of the noise from the later stages is reduced through the gain of the previous stages. In the following analysis, only the first transistor (M_1) and the input PIP network (L_{P1}–L_{P3} and R_{M1}–R_{M2}) are considered, as shown in Fig. 9. For 0.18-μm CMOS technology, previous studies indicate that the drain thermal noise dominates the device noise characteristics [19], [20]. Based on this conclusion, the mean-square noise current spectral density can be derived as

$$\begin{aligned}\overline{i_{n,in}^2} = {} & 4kTR_{M1}\left|\frac{1}{Z_{RL1}}\right|^2 \\ & + 4kTR_{M2}\left|\frac{1}{Z_{RL2}}+sL_{P3}\left(\frac{1}{Z_{RL1}Z_{RL2}}+\frac{sC_{pd}}{Z_{RL2}}\right)\right|^2 \\ & + \frac{4kT\gamma}{g_{m1}}\left|\frac{1}{Z_{RL1}}+\frac{1}{Z_{RL2}}+s(C_{pd}+C_{g1})\right. \\ & \left. +sL_{P3}\left(\frac{1}{Z_{RL1}Z_{RL2}}+\frac{sC_{g1}}{Z_{RL1}}\right.\right. \\ & \left.\left. +\frac{sC_{pd}}{Z_{RL2}}+s^2C_{pd}C_{g1}\right)\right|^2 \end{aligned} \tag{8}$$

where

$$\begin{aligned} Z_{RL1} &= R_{M1}+sL_{P1} \\ Z_{RL2} &= R_{M2}+sL_{P2} \end{aligned} \tag{9}$$

where γ is the noise factor of the drain thermal noise, and g_{m1} and C_{g1} are the transconductance and the equivalent gate capacitance of M_1, respectively. As can be seen from the equation, the capacitance related terms increase the noise current as the frequency increases, while the rest of the terms result in an opposite trend owning to the inductive reactance in the denominator. The measured results as will be shown in Section VI indicate that the in-band noise current decreases with increased frequency. In other words, the capacitance-related terms in (8) are not significant in the desired bandwidth. This trend can be attributed to the increased reactance of L with frequency, which provides relatively high impedances to block the noise currents generated from R_{M1}, R_{M2}, and M_1 to flow into the input terminal. Based on the above analysis, the PIP inductors at the input stage not only improve the bandwidth but also the noise performance in the desired band.

VI. Experimental Results

The TIA was fabricated in 0.18-μm CMOS technology with a chip area of 1.17×0.46 mm^2, as shown in Fig. 10. The TIA was measured on-wafer with coplanar ground-signal-ground (GSG) probes (Picoprobe 67A-GSG-125-C-W) for S-parameters, noise figure, and eye diagram measurements. Using the network analyzer 8510C, the S-parameters were taken from 0.1 to 40 GHz. The measured response of Z_T is shown in Fig. 11. The gain and

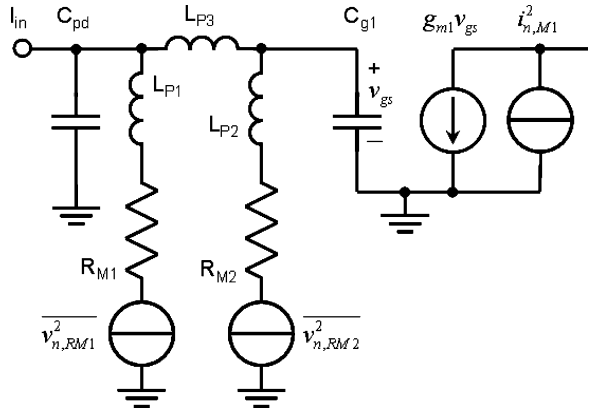

Fig. 9. Noise equivalent circuit model for the TIA input stage as shown in Fig. 7.

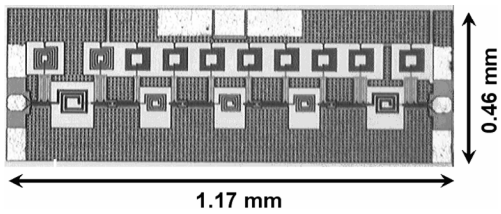

Fig. 10. Chip micrograph.

the 3-dB bandwidth $f_{3\mathrm{dB}}$ are 51 dBΩ and 30.5 GHz in the presence of an on-chip C_{pd} of 50 fF at the input, respectively. The magnitude of the input impedance Z_{IN} is 54 Ω at low frequencies, but increases due to the PIP inductors at around $f_{3\mathrm{dB}}$. The measured S_{22} within the $f_{3\mathrm{dB}}$ is all below −10 dB, and S_{21} at low frequencies is up to 16.7 dB, as shown in Fig. 12. The phase of Z_T is linearly decreased with frequency and the group delay variation is below 45 ps up to 24 GHz, as illustrated in Fig. 13. Note that a tradeoff exists between the bandwidth enhancement and the phase linearity. In this study, we mainly focus on bandwidth enhancement and thus the group delay variation increases. As will be observed from the eye diagrams of the TIA especially the one at 40 Gb/s [Fig. 16(d)], the signal smears and the rising and falling edges broaden due to the group delay variation with frequency, i.e., the phase velocity variation at different frequencies.

Using the noise figure analyzer N8975A, the noise figure (NF) was measured from 3.5 to 26.5 GHz, as shown in Fig. 14. The value decreases from 11.9 to 6.7 dB as the frequency increases, which is in an excellent agreement with the simulated results. The noise characteristic of the TIA can be represented by a single noise current source referred to the input [21]:

$$\overline{i_{n,in}^2} = \frac{\overline{v_{n,outamp}^2}}{Z_T^2} \tag{10}$$

where $v_{n,outamp}$ is the output noise voltage of the amplifier. Based on the definition of N_F, the noise current can be extracted as shown in Fig. 15. Note that the calculation is under a 50-Ω condition, which is consistent with the measurement environment. Also, the calculation includes the effect of the input capacitor C_{pd} connected in front of the TIA. As can be seen, a decreasing noise current with frequency can be observed and

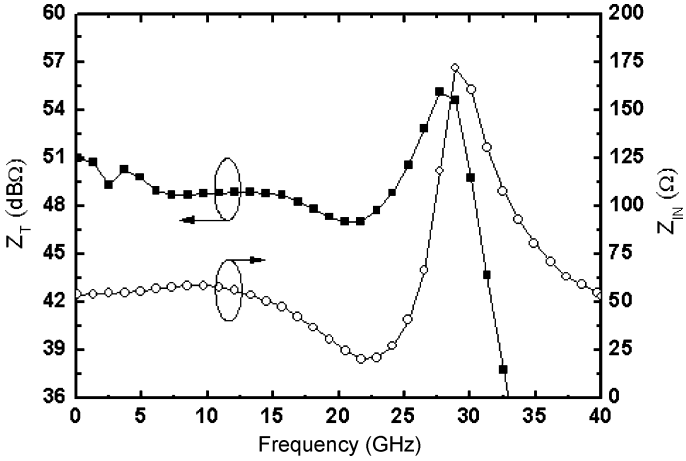

Fig. 11. Measured Z_T and $Z_{\rm IN}$.

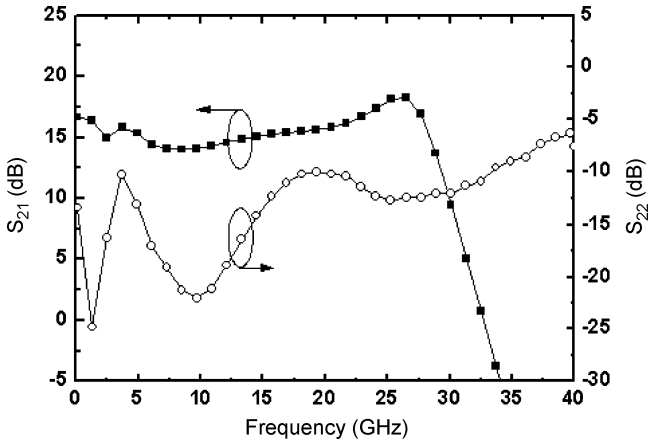

Fig. 12. Measured S_{21} and S_{22}.

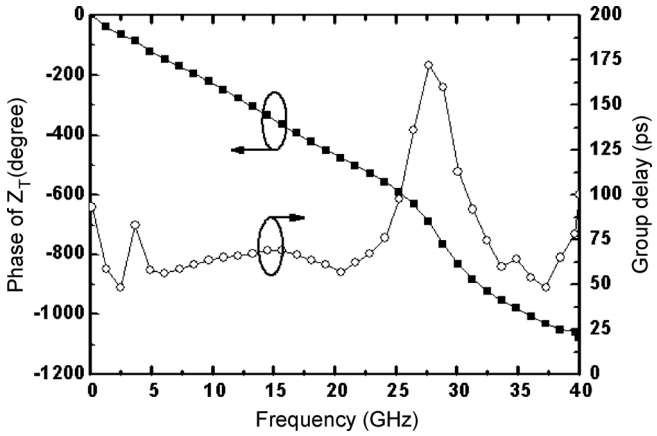

Fig. 13. Measured phase and group delay.

a lowest value of 34.3 pA/$\sqrt{\rm Hz}$ at 25 GHz is obtained. Although not measured directly, the simulated results indicate that the capacitance related higher order terms in (8) become significant only at above ~30 GHz. To investigate the effect of C_{pd} on the noise characteristic, the simulated $i_{n,in}$ with different C_{pd} values is presented in Fig. 15. As predicted by (8), the capacitance related terms increase the noise current as the

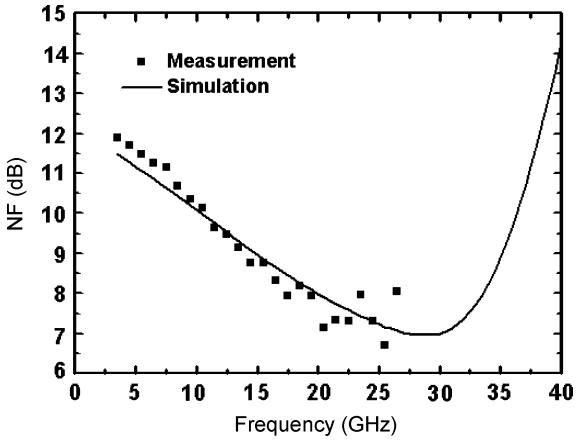

Fig. 14. Measured and simulated noise figure (NF).

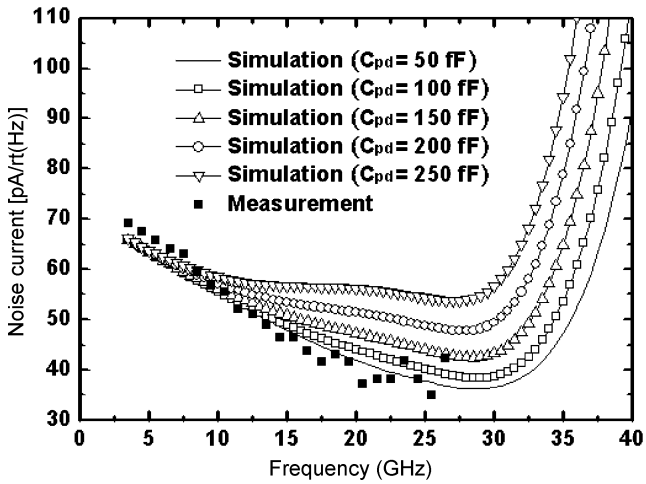

Fig. 15. Measured $I_{n,in}$ and the simulated $I_{n,in}$ with different values of C_{pd}.

frequency increases. When a large C_{pd} is applied, the C_{pd}-related terms become dominant and the noise current increases with frequency.

In addition, the root mean square (RMS) noise current can be calculated as [22]

$$i_{n,in}^{rms} = \frac{1}{R_T}\sqrt{\int_0^{>2f_{3-dB}} |Z_T(f)|^2 \cdot \overline{i_{n,in}^2}(f)df} \qquad (11)$$

where R_T is the midband value of Z_T. By integrating (11) up to 61 GHz $(2f_{\rm 3dB})$, the simulated $i_{n,in}^{rms}$ is 9.7 μA. A corresponding averaged noise current density of 55.7 pA/$\sqrt{\rm Hz}$ can be obtained from $i_{n,in}^{rms}/\sqrt{f_{\rm 3dB}}$, and the estimated sensitivity of the proposed TIA is 135.8 μA for a bit error rate (BER) of 10^{-12}. The comparison of the averaged noise current density with other 40-Gb/s TIAs is shown in Table II [7], [8]. In the proposed TIA, the gain of the first stage is somewhat small (~3.5 dB) resulting in a higher noise level when referred back to the input. The thermal noise generated from R_{M1} and R_{M2} which are optimized for wideband matching to a 50-Ω source termination is also a contributor to the input noise current.

To measure the transient response of the 40-Gb/s TIA, a $2^{31}-1$ PRBS is applied. The high-speed PRBS is generated from the multiplexer MP1803A using the 4-data-output pattern

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS

Ref.	BW (GHz)	Speed (Gb/s)	Z_T (dBΩ)	Z_{IN} (Ω)	S_{22} (dB)	Noise (pA/√Hz)	C_{pd} (fF)	Chip area (mm^2)	V_{DD} (V)	Power (mW)	GBP/P_{dc} (GHzΩ/mW)	Technology
This work	30.5	40	51	54	-10	55.7 (sim.)	50	1.17× 0.46	1.8	60.1	180.1	0.18-μm CMOS
[6]	30	40	48	—	—	—	—	0.8×1.3	1.8	50.4	149.5	0.18-μm CMOS
[23]	9.2	10	54	—	—	16.7 (sim.)	500	0.8×0.8	2.5	137.5	33.5	0.18-μm BiCMOS
[24]	8	10	53	—	—	18	250	0.6×0.6	1.8	13.5	264.7	0.18-μm CMOS
[25]	7.2	10	61	—	—	8.2	250	0.14	1.8	70.2	115.1	0.18-μm CMOS
[7]	42	40	59	35	-8	34.2	—	1×1	5.2	600	62.4	SHBT f_T= 150GHz
[8]	47	40	50	—	-10	29	—	0.675× 0.975	5.2	458	64.7	DHBT f_T= 160GHz
[9]	50	40	43	79*	-12	—	—	0.78× 1.18	5.2	182	38.8	SiGe f_T= 200GHz

* In the paper, S_{11}, S_{21}, and Z_T are -13 dB, 6.5 dB, and 43 dBΩ, respectively. The calculated $Z_{\rm IN}$ is 79 Ω.

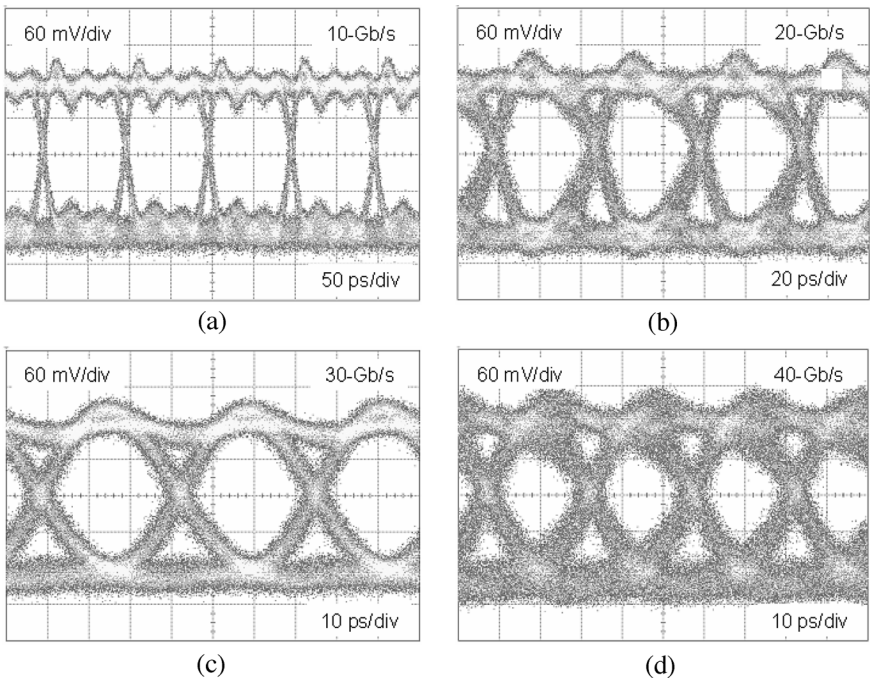

Fig. 16. Measured eye diagram with a $2^{31}-1$ PRBS input current of 740 $\mu A_{\rm pp}$ at (a) 10 Gb/s, (b) 20 Gb/s, (c) 30 Gb/s, and (d) 40 Gb/s.

generator MP1758A, and synchronized by the signal generator MG3695B. With an input current swing of 740 $\mu A_{\rm pp}$, the output eye diagrams at 10, 20, 30, and 40 Gb/s are shown in Fig. 16 with an output voltage swing of 263 $\rm mV_{pp}$.

With a 1.8-V supply voltage, the amplifier consumes 60.1 mW, and a gain–bandwidth product per DC power figure of merit $(\rm GBP/P_{dc})$ of 180.1 GHzΩ/mW is obtained. The circuit performance of the 40-Gb/s TIA is summarized in Table II together with four state-of-the-art 0.18-μm CMOS TIAs [6], [23]–[25] and three 40-Gb/s TIAs using SiGe and III-V technologies [7]–[9] published recently. As can be seen, the proposed TIA is comparable with those using the technologies with much higher f_T [7]–[9].

VII. CONCLUSION

In this paper, an effective bandwidth improvement technique has been demonstrated by a 0.18-μm CMOS TIA. The PIP technique can enhance the bandwidth of a cascaded CS stage by a factor of 3.31. The design concept was discussed in detail and the related equations were derived. Analyses of the noise current characteristics in the PIP configuration were also provided. From the measured results, the proposed circuit

presents a circuit bandwidth of 30.5 GHz and a $\mathrm{GBP}/P_{\mathrm{dc}}$ of 180.1 GHzΩ/mW.

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