A 1-V 45-GHz Balanced Amplifier With 21.5-dB Gain Using 0.18-μm CMOS Technology

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***Abstract*—A fully integrated balanced amplifier was realized in a standard 0.18-μm CMOS technology. From the measured S-parameters, a gain up to 21.5 dB was achieved at 45.4 GHz under a supply voltage of only 1 V and a total power consumption of 89 mW. An effective technique, i.e., π–type parallel resonance, was proposed to enhance the device and circuit frequency response. In addition, the semicoaxial line structure was used to reduce the signal loss and physical size of the Lange couplers in the amplifier. To the best of the authors' knowledge, the proposed balanced amplifier demonstrated the highest operation frequency and the lowest operation voltage among the published millimeter-wave amplifiers using a similar technology.**

***Index Terms*—Balanced amplifier, CMOS, Lange coupler, millimeter wave, parallel resonance, semicoaxial line.**

I. Introduction

THE BALANCED amplifier configuration was initially reported in 1965, and possesses many advantages such as a good input/output matching, a high degree of stability, and a 3-dB higher linearity [1], [2]. Composed of two identical sub-amplifiers and 90° couplers, the balanced configuration was employed extensively for millimeter-wave amplifiers by using III–V [3]–[5] or SiGe [6], [7] technologies. However, a fully integrated balanced amplifier based on the standard CMOS process for microwave applications has not been reported thus far. In this paper, a 45-GHz balanced amplifier realized in a 0.18-μm CMOS technology is successfully demonstrated. The designed frequency range has been used for satellite communication systems [8].

To design a high-performance balanced amplifier based on the standard CMOS technology, two issues need to be considered. One is that the high-frequency characteristic is, in general, not as good compared with the traditionally used III–V or SiGe transistors for the balanced amplifier. It is, therefore, a challenge to obtain a high-performance amplifier in the millimeter-wave frequency range. In addition, the commonly used Lange coupler in a microstrip form not only occupies a large chip area, but also introduces a considerable signal loss. In this study, two design techniques are employed to solve these problems. First, a novel π–type parallel resonance (PPR) topology is proposed, which can cancel out the inherent capacitances of the transistor through a parallel *LC* resonant network to increase the circuit gain and extend the operation frequency. Second, the semicoaxial line structure is employed [9], [10], which can effectively minimize the required chip area and reduce the signal loss of the Lange coupler. As a result, the proposed balanced amplifier achieves the highest operation frequency and gain compared to the state-of-the-art narrowband amplifiers using a similar technology [11]–[13].

Section II describes the design principles of the fully integrated balanced amplifier including the PPR and the semicoaxial Lange coupler. The measured results are presented in Section III, and Section IV concludes this study.

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II. Design of Balanced Amplifier

The circuit topology of the proposed CMOS balanced amplifier is shown in Fig. 1. The input signal is split into two paths by the input coupler with an ideally 3-dB insertion loss and a 90° phase difference. Two identical sub-amplifiers (SA1 and SA2) are used in each path to amplify the signal individually resulting in a 3-dB higher linearity. The two signals are then combined by the output coupler with an inverted 90° phase shift and delivered to the output terminal. As a consequence, the overall gain of the balanced amplifier is identical to that of the single sub-amplifier. If the input impedances of both sub-amplifiers are mismatched, the signals passing through the input coupler will be reflected back to the *input1* and the *isolated* ports with a 180° and 0° phase difference, respectively. The reflected signals at the *input1* port can be canceled, while those at the *isolated* port are absorbed by the termination resistor R_M. The same principle can be applied to the output coupler and output port. The S-parameters of a balanced amplifier can be represented by the S-parameters of the individual amplifiers [14]

$$|S_{11}| = 0.5\,|S_{11,SA1} - S_{11,SA2}| = 0 \tag{1}$$

$$|S_{12}| = 0.5\,|S_{12,SA1} + S_{12,SA2}| = S_{12,SA1} \tag{2}$$

$$|S_{21}| = 0.5\,|S_{21,SA1} + S_{21,SA2}| = S_{21,SA1} \tag{3}$$

$$|S_{22}| = 0.5\,|S_{22,SA1} - S_{22,SA2}| = 0. \tag{4}$$

By adopting the balanced configuration, excellent input and output matching conditions can be obtained simultaneously, while the gain and reverse isolation are kept unchanged.

In this design, each sub-amplifier consists of six common-source (CS) stages connected in a cascaded configuration to achieve a high gain under a low supply voltage. To isolate R_M and the input/output ports from the dc bias of the sub-amplifiers, four coupling capacitors C_C are utilized. The details of

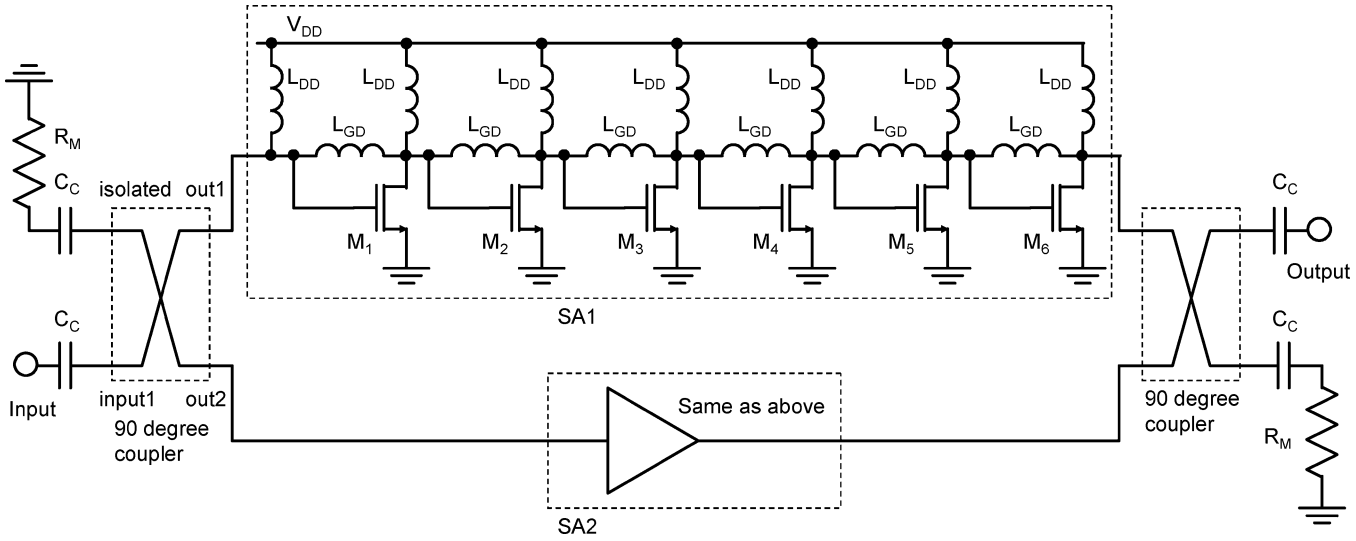

Fig. 1. Circuit topology of the fully integrated balanced amplifier. Two identical 90° couplers and sub-amplifiers (SA1 and SA2) are incorporated.

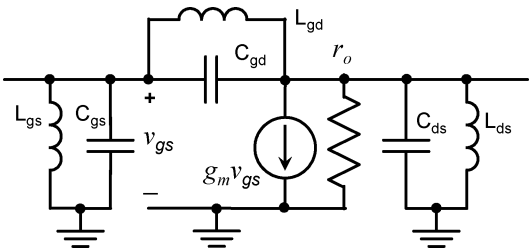

Fig. 2. Small-signal equivalent circuit model of a MOS transistor with PPR inductors.

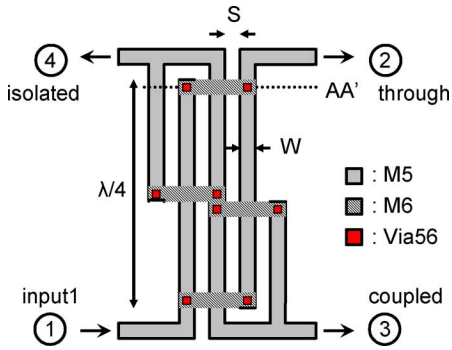

Fig. 3. Top-view of the Lange coupler in a standard 1P6M CMOS process.

the design for the fully integrated balanced amplifier are further described below.

A. PPR

As shown in Fig. 2, the small-signal equivalent circuit model of a MOS transistor can be simplified as a voltage-controlled drain current source $g_m v_{\rm gs}$, an equivalent small-signal output resistance r_o, a gate–source capacitance $C_{\rm gs}$, a gate–drain capacitance $C_{\rm gd}$, and a drain–source capacitance $C_{\rm ds}$. These inherent capacitances are the main limitation of the operation frequency for a MOS transistor. In this study, the PPR approach is proposed by inserting three inductors ($L_{\rm gs}$, $L_{\rm gd}$, and $L_{\rm ds}$) to individually resonate with the three capacitors in parallel to achieve a high gain performance at high frequencies. The required inductance can be determined by the following equation:

$$L = \frac{1}{C}(2\pi f_0)^2 \tag{5}$$

where f_0 is the center of the desired operation frequency band, C is the inherent capacitance, and L is the corresponding inductance. Each inherent capacitance can be estimated by extracting the small-signal equivalent circuit model of the transistor. For the cascaded CS stages, the drain–source inductor $L_{\rm ds}$ and the gate–source inductor $L_{\rm gs}$ of the next stage can be combined as one inductor L_{DD} shown in Fig. 1. With a frequency f_0 at the desired frequency, the designed L_{DD} and $L_{\rm GD}$ are 0.5 and 0.17 nH, respectively. Note that the total gatewidth of each transistor ($M_1 \sim M_6$) is 64 μm. The on-chip spiral inductors are designed by an electromagnetic (EM) simulator tool,[1] and the quality factors of 0.5- and 0.17-nH inductors are 5.1 and 8.8 at 45.4 GHz, respectively.

B. Semicoaxial Lange Coupler

The commonly used 90° couplers include the Lange coupler [3]–[5], [7] and the branch-line coupler [6]. In general, the former one occupies less chip area, while the latter one has a simpler structure. The Lange coupler is adopted in this design, which was realized by the metal layers for interconnection in a standard CMOS process. Fig. 3 shows the top view of the Lange coupler using the Metal 5 (M5) layer as the signal lines, while the Metal 6 (M6) layer is used as the crossover connections. The cross section of the coupler along the line AA', as indicated in Fig. 3, is shown in Fig. 4. In the 0.18-μm CMOS technology used here, one poly layer and six metal layers (1P6M) are available. The metal thickness t_m of M5 and M6 are 0.53 and 2.34 μm, respectively. Note that each layer has different values of the minimum metal width $W_{\rm min}$ and spacing $S_{\rm min}$, while the

[1]Sonnet Software, North Syracuse, NY. [Online]. Available: http://www.sonnetusa.com

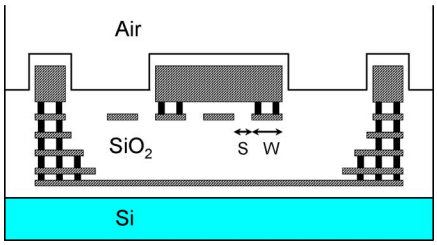

Fig. 4. Cross section of the semicoaxial Lange coupler along the dotted line AA', as indicated in Fig. 3.

two must be equal according to the design rule. The values of $W_{\min}(S_{\min})$ for M5 and M6 are 0.28 and 1.5 μm, respectively.

For Lange coupler design, the spacing S between the lines is an important consideration for signal coupling, while the metal width W is also a critical issue for signal loss. For the selection of the signal line layer, M6 is the best candidate for a low signal loss owing to a thicker t_m, while M5 is more suitable for high signal coupling due to a smaller $S_{\min}$. Based on the EM simulation , a better performance can be achieved by using M5 as the signal lines instead of using M6. The finally optimized values of S and W are 0.3 and 1.8 μm, respectively.

Another design challenge is to reduce the size of the coupler. The physical length of the Lange coupler is mainly limited by the quarter-wavelength ($\lambda/4$) line, as shown in Fig. 3, which not only occupies a large chip area, but also introduces a considerable amount of signal loss. In this study, a novel semicoaxial line structure using a standard CMOS process was employed to minimize the physical size and reduce the signal loss [9], [10], as shown in Fig. 4 for the cross section. With a high slow-wave factor, the physical size of the coupler is reduced, which can be attributed to the increased distributed inductance and capacitance resulting from the semirounded ground plane [10]. The shortened signal lines lead to a more area-efficient Lange coupler design with a reduced signal loss. Compared with the physical length (825 μm) of the conventional microstrip-type Lange coupler based on the same process, the length of the semicoaxial coupler is reduced by $\sim$27% to be only 600 μm.

The simulation results of the semicoaxial Lange coupler are shown in Fig. 5. Over a wide frequency range (40 $\sim$ 50 GHz), the insertion losses of S_{21} and S_{31} are approximately 5 dB, and the phase difference between ports 2 and 3 is approximately 90°. In addition, the input reflection S_{11} and isolation S_{14} are both below -10 dB in the desired frequency range.

C. Simulated Results of the Balanced Amplifier

Fig. 6(a) and (b) shows the simulated S-parameters of both the individual amplifier SA1 in one branch and the overall balanced amplifier. As can be seen, SA1 was designed to have a high gain while not considering the input/output matching conditions. By adopting the balanced configuration with the couplers, as predicted in (1) and (4), the reflection coefficients are greatly improved to be below -10 dB over a wide frequency range. The results also indicate an unconditional stability even under such a high gain condition. Note that the gain is dropped by $\sim$ 4 dB at the peak-gain frequency f_p for the balanced amplifier due to the additional loss of the couplers.

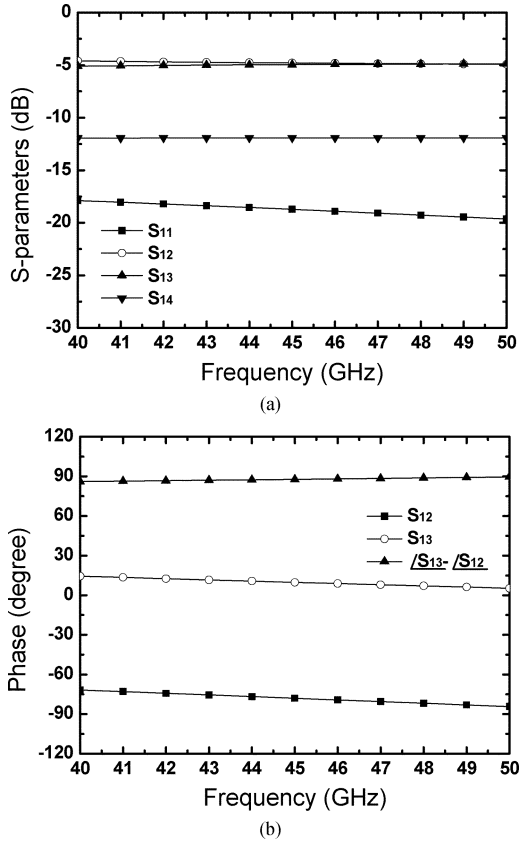

Fig. 5. Simulated frequency responses of the semicoaxial Lange coupler in: (a) magnitude and (b) phase.

The simulated noise figure (NF) of the proposed balanced amplifier is shown in Fig. 7. The NF is 12.8 dB at 45.4 GHz. Note that the NFs contributed from the input coupler and the sub-amplifier are 2.1 and 10.5 dB, respectively. The noise performance may be further improved by carefully optimizing the transistor sizes, especially the first gain stage M_1. Although the NF is relatively high, this amplifier can be useful as a gain block with a low-noise amplifier connected in front.

III. Measured Results

The proposed balanced amplifier was realized in a standard 0.18-μm CMOS process with a physical size of 0.63×0.96 mm^2 including the probing pads (core area: 0.53×0.76 mm^2), as shown in Fig. 8. The semicoaxial structure was also utilized for on-chip interconnects and probing pads to reduce the signal loss and crosstalk. It may also be noticed in Fig. 8 that the 0.17-nH inductor is realized by one on-chip inductor only. However, the 0.5-nH inductor is implemented by three on-chip inductors connected in series to shorten the distance between the two transistors. Note that the distances between the inductors have been carefully arranged to reduce the coupling effect by EM simulation . The chip was measured on-wafer with the coplanar ground–signal–ground (GSG) probes (Picoprobe 67A-GSG-125-C-W). Using the network analyzer 8510C, the S-parameters were taken from 40 to 50 GHz, as shown in Figs. 9 and 10 together with the simulated results. With a measured peak gain G_p of 21.5 dB at f_p of 45.4 GHz, the measured S_{11} and S_{22} are -13.0 and -14.9 dB, respectively. The measured

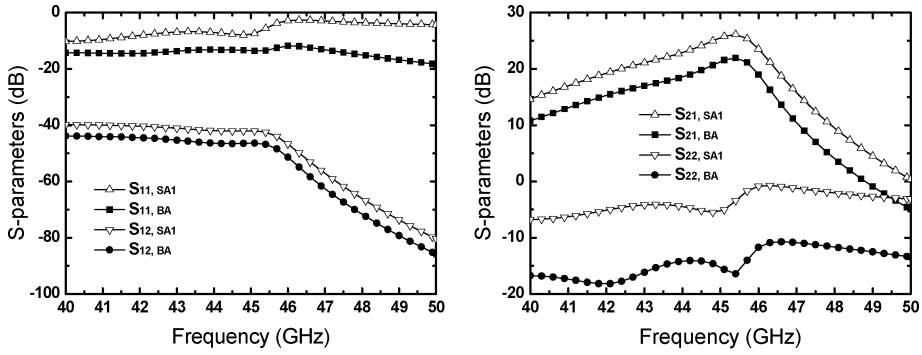

Fig. 6. Simulated: (a) S_{11} and S_{12} and (b) S_{21} and S_{22} of the balanced amplifier (BA) and SA1.

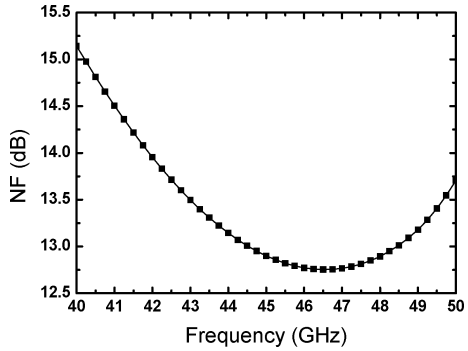

Fig. 7. Simulated NF of the balanced amplifier.

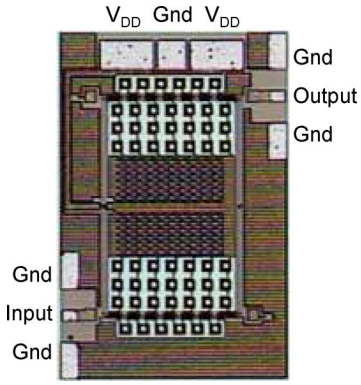

Fig. 8. Chip micrograph of the CMOS balanced amplifier. (0.63×0.96 mm^2, including probing pads).

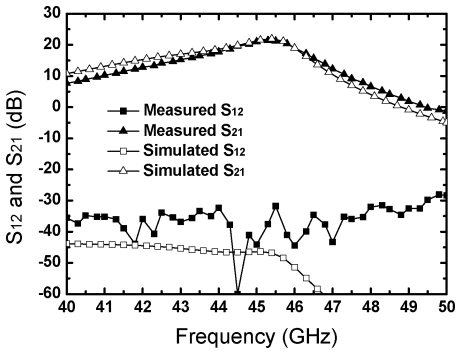

Fig. 9. Measured and simulated S_{12} and S_{21} of the proposed CMOS balanced amplifier.

3-dB bandwidth is in a range of 44.2–46.1 GHz. Deviations between the simulated and measured results can be mainly attributed to the inaccuracy of the foundry provided equivalent

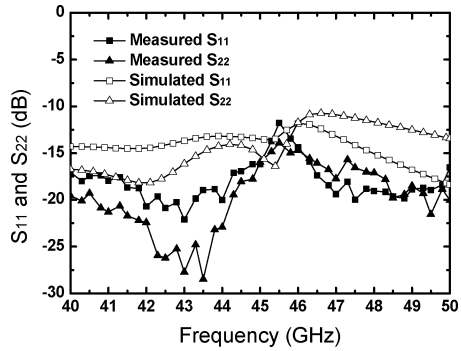

Fig. 10. Measured and simulated S_{11} and S_{22} of the proposed CMOS balanced amplifier.

TABLE I
SUMMARY OF THE STATE-OF-THE-ART NARROWBAND AMPLIFIER PERFORMANCES

Ref.	This work	[11]	[12]	[13]	[16]
f_p (GHz)	45.4	40.0	32.0	25.7	40
G_p (dB)	21.5	7.0	10.2	8.9	19
S_{11} (dB)	-13.0	-15.0	-13.3	-14.0	-15.0
S_{22} (dB)	-14.9	-15.0	-13.4	-12.0	-15.0
3-dB gain BW (GHz)	44.2-46.1	–	–	–	34-44
V_{DD} (V)	1	3	1.8	1.8	1.5
P_{DC} (mW)	89	300	27	54	36
$G_p f_p/P_{DC}$ (GHz/mW)	6.06	0.30	3.84	1.33	9.90
Chip area (mm^2)	0.63x 0.96	1.2x 1.7	0.74x 0.5	1.05x 0.7	1.3x 1.1
Number of stage	6	3	3	3	3
Process	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.13μm CMOS

circuit models, which are verified only to 20 GHz. On the other hand, the EM simulation results are verified up to 50 GHz for the customized inductors and couplers. A high peak gain-frequency product per dc power $G_p f_P/P_{\rm DC}$ of 6.06 GHz/mW is achieved under a supply voltage of 1 V and a total power consumption $P_{\rm DC}$ of 89 mW. The circuit characteristics are summarized in Table I together with the state-of-the-art millimeter-wave amplifiers using a similar technology [11]–[13]. Among them, this study achieves the highest operation frequency, gain,

and $G_p f_P / P_{\rm DC}$ under the lowest operation voltage. Compared with the amplifier realized by a more advanced technology [15], this design presents a higher gain and consumes a smaller chip area under a lower supply voltage.

IV. Conclusion

By using two effective design techniques, a 45-GHz balanced amplifier with a 21.5-dB gain was demonstrated in a 0.18-μm CMOS technology. Under a supply voltage of only 1 V, a high $G_p f_P / P_{\rm DC}$ of 6.06 GHz/mW was achieved. By adopting the newly proposed PPR technique, the operation frequency was extended by canceling out the inherent capacitances of a MOS transistor through parallel *LC* resonance. In addition, the semi-coaxial structure was employed for the Lange coupler design, and the physical length was reduced by a factor of $\sim$27% compared with that realized by the conventional microstrip lines.

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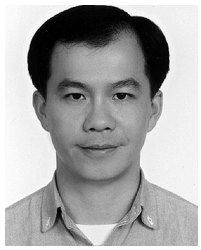

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