A Wide Locking-Range Frequency Divider for LMDS Applications

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***Abstract*—A fully integrated frequency divider with an operation frequency up to 20 GHz is designed in 0.18-μm CMOS technology. The frequency divider includes two stages to divide the input signal by a factor of 4. A wide locking range from 18.8 to 23.2 GHz was obtained with a low phase noise of -134.8 dBc/Hz (1-MHz offset) at an output frequency of 4.7 GHz. The first stage is designed by an analog methodology with the varactors to extend the locking range, while the second stage is designed by a digital approach with the RF devices for a high operation frequency. With the advantages of both designs, this frequency divider is operated at the frequency range suitable for LMDS applications.**

***Index Terms*—Analog circuits, CMOS RF circuits, digital circuits, divider circuits.**

I. Introduction

THE demand for broadband and high data rate transmission increases the operation frequency of communication systems rapidly. Local multipoint distribution systems (LMDS) [1], [2] is a system which employs a point-to-multipoint broadcast downlink with a total capacity of 34–38 Mb/s per transport stream for digital TV broadcast and consumer entertainment services. LMDS typically operates at millimeter-wave frequencies of above 20 GHz [3]. In this work, a frequency divider operating in the frequency range suitable for such applications with a function of /4 is realized by a stand 0.18-μm CMOS technology. The circuit topology contains two stages: the first stage is an analog frequency divider with low power consumption and high operation frequency, while the second stage is a digital frequency divider with RF transistors for both high frequency and a small chip area. A wide locking range from 18.8 to 23.2 GHz was obtained with an overall power consumption of 38.7 mW.

Section II describes the operation principle and schematic of the two stages, respectively. In addition, the comparison of the devices for RF and digital applications, and the impact of process variation on circuit performance are addressed. Section III presents the measurement results and the conclusions are made in Section IV.

II. Design of Frequency Divider

A. First-Stage Design

The first stage of the frequency divider is shown in Fig. 1, which is designed based on the concept of an injection-locked frequency divider (ILFD) [4]–[8]. Compared with the widely used current-mode logic (CML) divider [9]–[11], and the ILFD provides an alternative choice to achieve low power consumption and high operation frequency simultaneously. The ILFD configuration used here is similar to a cross-coupled pair voltage-controlled oscillator with the input signal injected from the bottom current source. This topology has a nature tendency of dividing input frequency by 2 [12]. The free-running frequency f_{fr} of the divider is designed at about half of the input signal frequency f_0. Since the second harmonic signal dominates at node V_x (the fundamental frequency f_{fr} is canceled at this node), the signal frequency at this node is locked to the input signal after the locking process. As a result, the frequency of the signal taken from the output $(V_{\text{out}+}, V_{\text{out}-})$ of the divider is half of the input signal V_{input}.

The locking range of the frequency divider can be estimated by the circuit parameters as shown below [4], [5]

$$\left|\frac{\Delta\omega}{\omega_r}\right| \leq \left|\frac{H_0 a_2 V_1}{2Q}\right| \tag{1}$$

where $\Delta\omega$ is the locking range, Q is the quality factor of the *LC* tank, ω_r is the resonant frequency, H_0 is the coefficient of the transfer function of the *LC* tank, a_2 is the coefficient of a third-order nonlinear equation for the *LC* oscillator (i.e., $f(e) = a_0 + a_1 e + a_2 e^2 + a_3 e^3$), and V_i is the amplitude of the incident signal. As can be seen, the locking range is inversely proportional to the quality factor of the *LC* tank, therefore an inductor or a capacitor with a smaller quality factor can increase the locking range. Simulations indicate that the inductors used in this design have a quality factor about 15 in the operation frequency range. In addition, the accumulation-typed varactors with a quality factor about 10 were employed in the *LC* tank to increase the locking range.

In order to drive the second stage, the amplitude of the output signal of the first stage needs to be larger enough, which is about 1.1 V in this case. The sizes of transistors M1 and M2 are designed to have sufficient output swing and minimize the loss of the parasitic capacitances. The finally selected width of both devices is 2.5 μm with 15 fingers.

B. Second-Stage Design

As also shown in Fig. 1, the second stage of the frequency divider employs a digital design approach consisting of transmission gate and inverters. With only one transmission gate at the input [13], this configuration can reach a higher operation frequency compared with the conventional structure.

Fig. 2 presents the time diagram of the second-stage digital divider, which illustrates the operation principle of the second-stage divider. By designing a proper propagation delay for each

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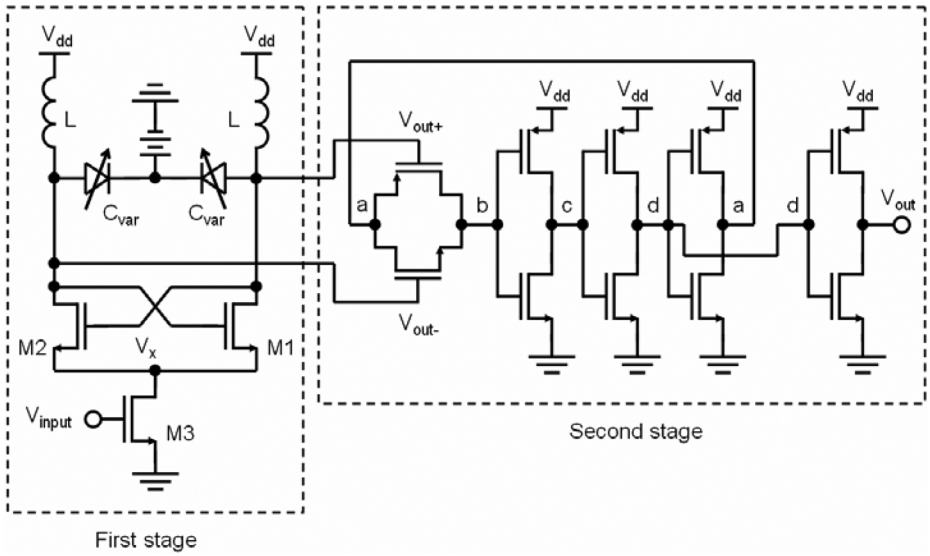


Fig. 1. Circuit schematic of the proposed two-stage frequency divider.

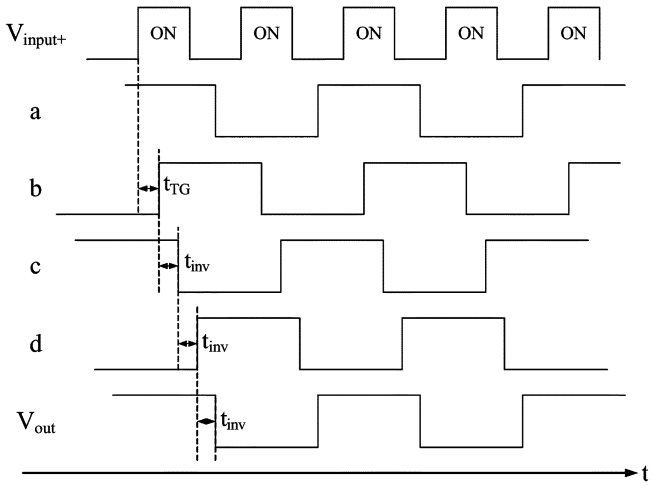


Fig. 2. Time diagram for the second stage of the proposed frequency divider.

stage, this circuit can function correctly as a frequency divider. First, assuming the logic state of node a starts as 1, when the transmission gate is on, the state of node b becomes 1 after a propagation delay of the transmission gate. Then the state of node c becomes 0 after a delay time of the inverter, and the other nodes also follow the same rule to change the states. Based on Fig. 2, with a proper propagation delay of each stage, the period of $V_{\rm out}$ is twice of that for the input signal. In other words, this circuit divided the frequency of the input signal by a factor of 2.

The locking range of the second stage can be determined by (2) with the delay time of the inverter $(t_{\rm inv})$ and the transmission gate $(t_{\rm TG})$, where n is the stages of the inverter. For a correct operation of the digital divider, the voltage level of node a needs to change within the off period of the transmission gate [13]. According to (2), with less stages of the inverter, the frequency divider can operate at higher frequencies

$$\frac{1}{2\times(t_{\rm TG}+n\cdot t_{\rm inv})}\le \text{locking range}\le \frac{1}{(t_{\rm TG}+n\cdot t_{\rm inv})}. \tag{2}$$

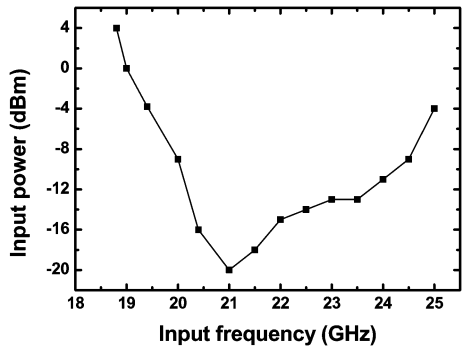


Fig. 3. Simulated results of the sensitivity (input power) as a function of the locking range (input frequency).

Note that the differential output of the first stage can be used as the input signal for the second stage directly without any buffer stages.

Fig. 3 shows the simulated sensitivity (input power) as a function of the locking range (input frequency). As can be seen, the locking range is ∼18.8–25.0 GHz with the best sensitivity at 21 GHz, which is about two times of the free-running frequency of the first-stage ILFD.

C. Device Considerations

As mentioned, the second-stage divider is designed based on a digital circuit topology, however, the RF devices were employed in the design to increase the operation speed and reduce noise coupling between different blocks especially operating at such a high frequency. Fig. 4(a) and (b) compares the conventional digital and the typical RF layouts for the nMOS devices with a finger number of 12 and the width of each finger of 6 μm in a 0.18-μm technology. The chip sizes are also labeled in the figures. Note that two dummy gates are added at each side of the RF device to reduce the process variation. The layout of the RF transistor has been optimized for high frequency applications, which is surrounded by a deep N-well to prevent the noise coupling from substrate and reduce the parasitic capacitance and resistance at high frequencies. In addition, the poly gates of the

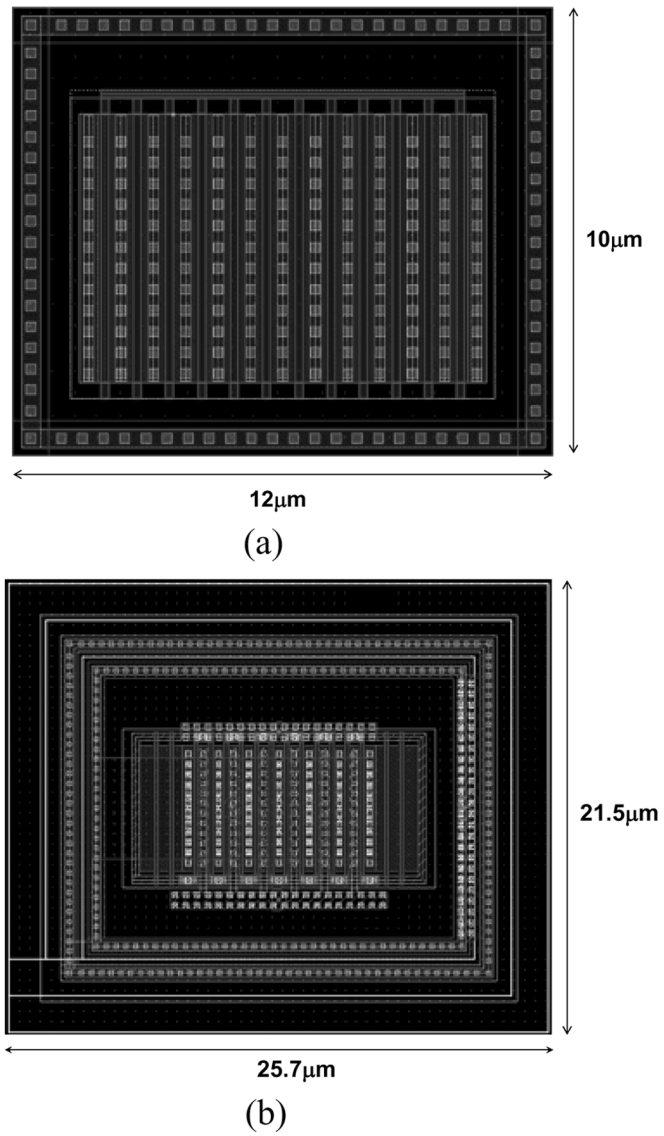


Fig. 4. (a) Layout of the conventional digital device (0.18 μm $\times$ 6 μm $\times$ 12). (b) Layout of the RF device (0.18 μm $\times$ 6 μm$\times$ 12).

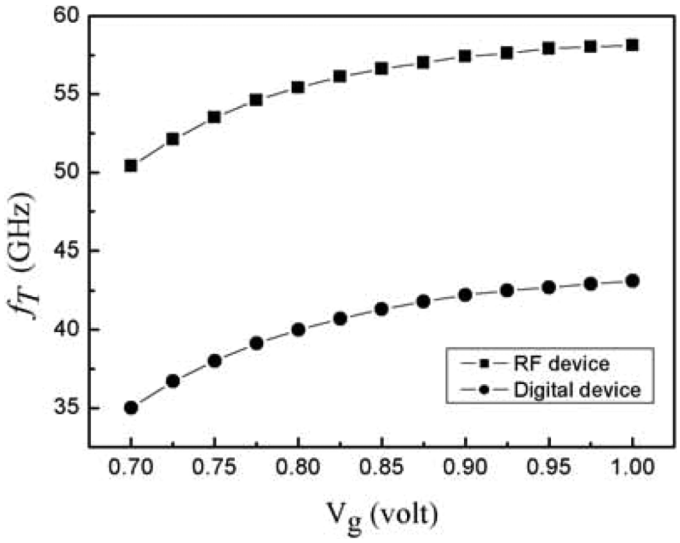


Fig. 5. Unit current gain frequency f_T of the RF and digital devices as a function of V_g. The drain voltage is fixed at 1 V.

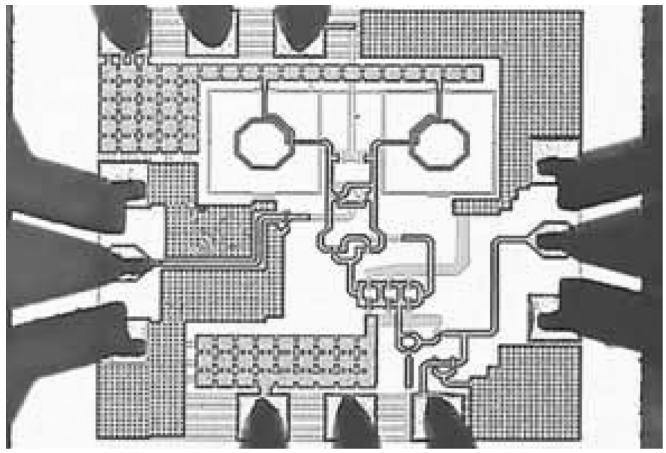


Fig. 6. Die photograph of the proposed frequency divider.

transistor are designed as a meander type and surrounded by metal 2 to reduce the overall gate resistance. Note that the minimum rules of the contacts are carefully applied to reduce the parasitic capacitance introduced by the overlapped metal layers in the RF devices. As a result, the operation frequency can be increased effectively compared to a device with a typical digital device layout under the same bias condition.

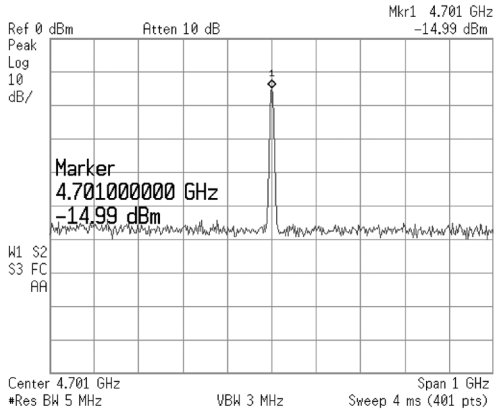
Fig. 5 compares the simulated results of the unit current gain frequency f_T for both the RF and digital nMOS devices corresponding to Fig. 4 as a function of the gate voltage V_g under a fixed drain-source bias of 1.0 V. As can be seen, the f_T of the RF device is substantially higher than that of the digital device under the same gate bias voltage. The designed digital frequency divider with RF devices demonstrates an operation frequency up to 11.6 GHz, which can be mainly attributed to the optimized layout of the RF CMOS devices. It can be seen that a trade-off exists between the device performance and the size. However, the overall chip area is dominated by the passive inductors and the RF probing pads, which can be seen from the circuit micrograph in Fig. 6 as will be shown later.

The device mismatch effect is also studied here for the propagation delay of the second stage. The simulation of the corner cases for fast–fast (FF) and slow–slow (SS) were both performed. For example, at the input signal of 10 GHz of this stage, compared to the typical–typical (TT) case, the transmission gate delay $t_{\rm TG}$ and the inverter delay $t_{\rm inv}$ both reduced by 19% for the FF case, while $t_{\rm TG}$ and $t_{\rm inv}$ increased by 9.5% and 14.3%, respectively, for the SS case. However, the divider can still function properly in these corner cases. As described in Section II-B, the divider can work correctly as long as the status of node a changed within the off period of the transmission gate, which provides a considerable tolerance, and is typically larger than the delay variation introduced by the transistor mismatch.

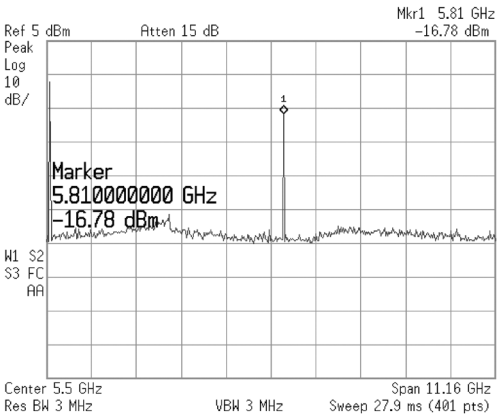
In addition, the impact of the device mismatch on the tuning range of the divider was carried out. The simulated result shows a locking range of 18.8–25 GHz for the TT case. For the corner cases of FF and SS, the simulated results show that the locking ranges change to 20.8–25.5 GHz and 18.8–22.5 GHz, respectively. The change in the locking ranges in both cases can be mainly attributed to the first-stage analog divider, which is more

TABLE I
COMPARISON WITH OTHER PUBLISHED FREQUENCY DIVIDERS

	This work	[7]	[14]
Operating frequency (GHz)	23.2	40	20
Locking range (GHz)	4.4	2.3	0.15
Power consumption(mW)	38	31	12.5
Supply voltage(Volt)	1.8	2.5	2.0
Technology	0.18-μm CMOS	0.18-μm CMOS	0.13-μm CMOS
FOM (GHz/W)	116	74	12



(a)



(b)

Fig. 7. (a) Output signal is 4.7 GHz with an input signal of 18.8 GHz. (b) Output signal is 5.81 GHz with an input signal of 23.2 GHz.

sensitive to the process variation. The second-stage digital divider, as analyzed above, is not strongly depend on the transistor mismatch effect in our design even with the delay variation introduced in the corner cases.

III. MEASUREMENT RESULTS AND COMPARISON

The proposed frequency divider was manufactured by TSMC 0.18-μm CMOS technology. The die photograph is shown in Fig. 6. The chip size including the RF probing pad is $0.82 \times 0.83\text{mm}^2$, while the core size of the circuit is about 0.5×0.53 mm^2. As can be seen on the left side, the grounded-coplanar-waveguide (GCPW) structures are employed at the input port to further reduce the signal loss and undesired noise coupling for high frequency operation.

Measurement was performed by an Agilent E4407B spectrum analyzer. With a function of divided by 4, the output signal is 4.7 GHz when the input signal is 18.8 GHz as shown in Fig. 7(a). Fig. 7(b) shows the measured output signal of 5.81 GHz with an input signal of 23.2 GHz. The measured phase noise is -134.8 dBc/Hz at 1-MHz offset as shown in Fig. 8. The measured results demonstrated the proposed frequency divider with a wide locking range from 18.8–23.2 GHz under a fixed input power level of ~ 5 dBm, and a function of divided by 4. The locking range obtained from the measurement is close to the simulated result of 18.8–25.0 GHz.

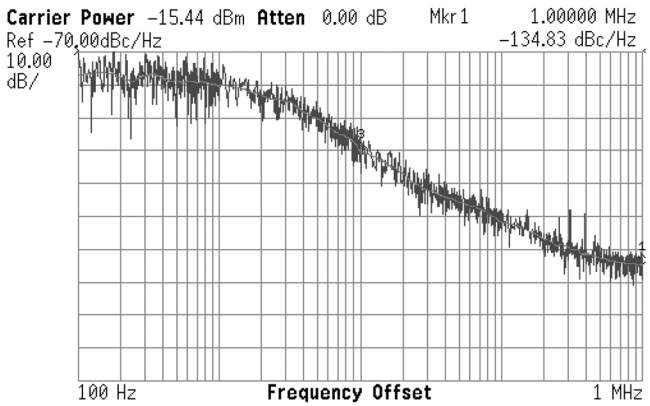


Fig. 8. Measured phase noise of -134.8 dBc/Hz at a 1-MHz offset (output frequency is 4.7 GHz).

Table I compares this work with recently published results by CMOS technology [7], [14]. The proposed circuit presents the widest locking range among these results. A figure-of-merit (FOM) is defined as the locking range divided by the total power consumption for a fair comparison, which is also listed in Table I.

IV. CONCLUSION

In this study, a frequency divider with a function of divided by 4 was implemented in a 0.18-μm CMOS technology. The circuit can operate up to 23.2 GHz with a locking range of 4.4 GHz, which consists of both analog and digital circuits with advantages from both design concepts. The proposed frequency divider use varactors to increase the locking range and the RF devices in the second stage to increase the operation frequency. Compared with other works, this circuit has the widest locking range among the published results. The proposed frequency divider is suitable for LMDS applications.

REFERENCES

[1] A. Nordbotten, "LMDS systems and their application," *IEEE Commun. Mag.*, vol. 38, no. 6, pp. 150–154, Jun. 2000.

[2] S. Y. Seidel, "Radio propagation and planning at 28 GHz for local multipoint distribution service (LMDS)," in *Proc. IEEE Antennas Propagation Soc. Int. Symp.*, Jun. 1998, vol. 2, pp. 622–625.
[3] H. Sari, "Some design issues in local multipoint distribution systems," *IEEE Signals, Syst. Electron.*, pp. 13–19, Sep. 1998.
[4] H. R. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 813–821, Jun. 1999.
[5] H. R. Rategh and T. H. Lee, "Superharmonic injection- locked oscillators as low power frequency dividers," in *Dig. Symp. VLSI Circuits* , 1998, pp. 132–135.
[6] A. Mirzaei, "Transient analysis of injection-locked frequency dividers," in *Proc. IEEE Midwest Symp. Circuits Syst.*, Aug. 4–7, 2002, vol. 3, pp. 381–384.
[7] J. Lee and B. Razavi, "A 40-GHz frequency divider in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 594–601, Apr. 2004.
[8] A. Safarian, S. Anand, and P. Heydari, "On the dynamics of regenerative frequency dividers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 12, pp. 1413–1417, Dec. 2006.
[9] W. Liu, S. Liu, and S. Wei, "CMOS current-mode divider and its applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 3, pp. 145–148, Mar. 2005.
[10] M. Alioto, R. Mita, and G. Palumbo, "Design of high-speed power-efficient MOS current-mode logic frequency dividers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, pp. 1165–1169, Nov. 2006.
[11] P. Heydari and R. Mohanavelu, "A 40-GHz flip-flop-based frequency divider," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 12, pp. 1358–1362, Dec. 2006.
[12] H. R. Rategh, H. Samavati, and T. H. Lee, "A CMOS frequency synthesizer with an injection-locked frequency divider for a 5-GHz wireless lan receiver," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 780–787, May 2000.
[13] M. Nogawa and Y. Ohtomo, "A 16.3-GHz 64:1 CMOS frequency divider," in *Proc. IEEE Asia Pacific Conf.*, Aug. 2000, pp. 95–98.
[14] F. H. Huang, D. M. Lin, H. P. Wang, W. Y. Chiu, and Y. J. Chan, "20 GHz CMOS injection-locked frequency divider with variable division ratio," in *Proc. IEEE RFIC Symp.*, Jun. 2005, pp. 469–472.