Low-Loss Differential Semicoaxial Interconnects in CMOS Process

Jun-De Jin, Shawn S. H. Hsu, *Member, IEEE*, Ming-Ta Yang, *Associate Member, IEEE*, and Sally Liu

***Abstract*—Design, characterization, and modeling of differential semicoaxial interconnects based on a standard 0.18-μm CMOS process are presented for the first time. The differential semicoaxial line shows a low differential-mode attenuation constant of ~1.00 dB/mm at 50 GHz and a slow-wave factor above 3.1 over a wide frequency range. The characteristics of differential semicoaxial lines for differential mode, common mode, slow-wave effect, and coupling effect are also investigated in details based on the measured mixed-mode S-parameters. The lumped $RLGC$ circuit is adopted to model the CMOS differential semicoaxial lines. An excellent agreement between the measured and modeled results is obtained up to 50 GHz.**

***Index Terms*—CMOS, differential line, lumped $RLGC$, mixed-mode S-parameters, semicoaxial interconnects.**

I. Introduction

THE ADVANCED CMOS technologies have dramatically increased the operation frequency of Si-based differential monolithic microwave integrated circuits (MMICs) [1], [2]. In the scope of circuit design, the differential topology features advantages of low common-mode noise, large output power, and small even-order harmonics. However, without careful design, the differential interconnects in the circuit can degrade the overall circuit performance, especially at high frequencies.

The commonly used interconnect structures for microwave circuits are the microstrip line [3], [4] and coplanar waveguide (CPW) [4]–[6]. For Si-based integrated circuits (ICs), however, they may not be the best candidates due to the crosstalk and loss of the lines [7]. In this study, low-loss differential interconnects with a semicoaxial structure are realized by utilizing the multiple metal layers in modern CMOS process. With a semirounded ground plane, the differential semicoaxial line structure can be expected to reduce the crosstalk from the adjacent interconnects and the loss introduced by the lossy Si substrate.

The concept of semicoaxial structure has been reported in [8], but only with simulated results for single semicoaxial lines in the silicon-on-insulator (SOI) process. For differential semicoaxial lines in standard CMOS technologies, a preliminary investigation has been reported by the authors [9]. In this study, a more detailed analysis on the slow-wave effect, coupling effect, and modeling of the differential semicoaxial lines will be presented. These topics have not been analyzed and discussed for CMOS-based differential lines, which also provide useful information for the interconnect design and optimization for Si-based differential ICs. Section II compares various interconnect structures and describes the design of differential semicoaxial lines. Section III presents and discusses the measured characteristics of differential semicoaxial lines for both the differential and common modes. In addition, slow-wave and coupling effects are investigated in details based on the mixed-mode S-parameters [10], [11]. Section IV focuses on the modeling of differential semicoaxial lines by utilizing the lumped $RLGC$ equivalent circuit, and Section V concludes this study.

II. Analysis and Design of Differential Semicoaxial Interconnects

Three differential-interconnect structures in the CMOS process are shown in Fig. 1, and the pros and cons are summarized in Table I. For the differential microstrip and differential semicoaxial lines, the lossy Si substrate is shielded by the bottom metal layer. On the other hand, the differential CPW suffers more from the loss introduced by the lossy Si substrate, which is referred to as substrate skin effect [7].

Regarding the crosstalk reduction, the differential microstrip line is relatively poor due to no ground planes existed between the signal lines for coupling isolation, while that of the differential semicoaxial line is excellent since the sidewall and bottom ground planes significantly alleviate the crosstalk through the SiO_2 layer and Si substrate, respectively. The crosstalk of the differential CPW is between the other two structures due to the presence of substrate coupling. The above qualitative analysis suggests that the differential semicoaxial line is the best structure among the three interconnects. These trends have also been verified by electromagnetic (EM) simulations.

The designed differential semicoaxial lines were fabricated in a standard one-poly and six-metal layers (1P6M) 0.18-μm CMOS process. The signal line was realized by the top-metal layer (M6) with a thickness of 2.34 μm, while the semirounded ground planes were designed by the multiple metal layers from M2 to M6, as shown in Fig. 1(c). The geometries, except the width (W_{tg}) of the top ground plane, were designed by the empirical equations for characteristic impedance (Z_0) [12] with three different Z_0 of 33, 50, and 75 Ω, as summarized in Table II. The W_{tg} was designed the same as signal width (W_s). The

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J.-D. Jin and S. S. H. Hsu are with the Department of Electrical Engineering and Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan 300, R.O.C. (e-mail: d929003@oz.nthu.edu.tw; shhsu@ee.nthu.edu.tw).

M.-T. Yang and S. Liu are with the Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan 300-77, R.O.C. (e-mail: mtyang@tsmc.com; s_liu@tsmc.com).

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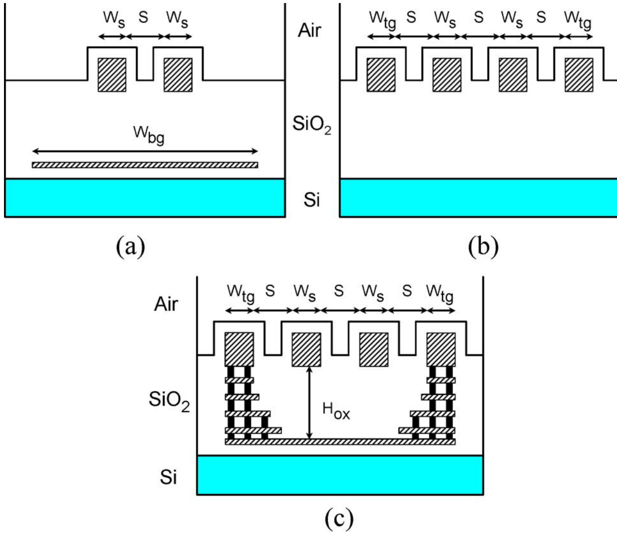

Fig. 1. Microwave interconnect structures for: (a) differential microstrip line, (b) differential CPW, and (c) differential semicoaxial line in a standard 1P6M 0.18-μm CMOS process. (Color version available online at http://ieeexplore.ieee.org.)

TABLE I
COMPARISON OF VARIOUS CMOS MICROWAVE INTERCONNECT STRUCTURES

	Differential microstrip line	Differential CPW	Differential semi-coaxial line
Si substrate shielding	Excellent	Poor	Excellent
Crosstalk reduction	Poor	Medium	Excellent

TABLE II
GEOMETRIES OF DESIGNED DIFFERENTIAL SEMICOAXIAL LINES ($H_{\rm ox} = 6.52$ μm, $l = 400$ μm. FROM [9]

	W_s (μm)	S (μm)	W_{tg} (μm)	Z_0 (Ω)
D-SC1	15	2.4	15	33
D-SC2	15	79.5	15	50
D-SC3	5	2.4	5	50
D-SC4	5	10.8	5	75

length (l) of all differential semicoaxial lines is 400 μm due to the limited chip area.

III. MEASUREMENT RESULTS AND DISCUSSION

The differential semicoaxial lines were measured on-wafer with Cascade coplanar ground–signal–ground–signal–ground (GSGSG) infinity probes and an Agilent E8364A four-port PNA network analyzer from 0.2 to 50 GHz. For the Si-based interconnect measurements, deembedding becomes a critical issue due to the low signal level and the lossy Si substrate. In this study, the ground shielded test structure was employed [13] and the pads area was minimized to 50 $\times$ 50 μm^2 both to improve the deembedding accuracy. Fig. 2 shows the micrograph of line D-SC4.

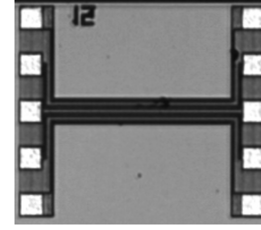

Fig. 2. Micrograph of line D-SC4. The area of each probing pads is 50 $\times$ 50 μm^2.

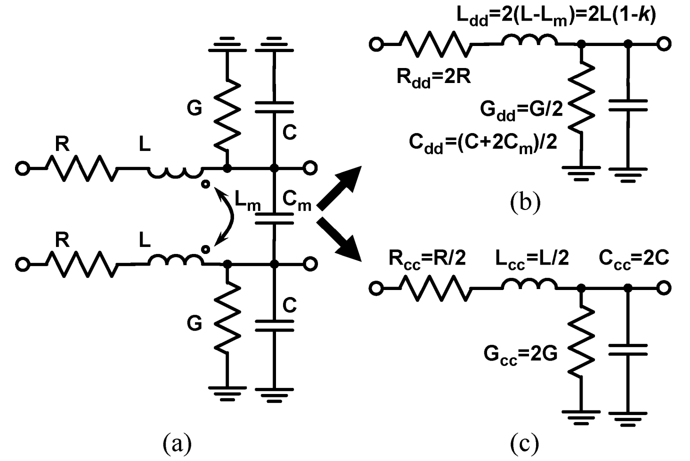

Fig. 3. Lumped-element $RLGC$ circuit model with one section for a symmetric differential line. (a) Four-port model. (b) Differential mode. (c) Common mode. From [9].

A. Four-Port Circuit Model

The four-port lumped-element circuit model of a symmetric differential line is depicted in Fig. 3(a), which includes the coupling effects between the two signal lines. The mutual inductance (L_m) and capacitance (C_m) per unit length describe the current and voltage coupling, respectively. R, L, G, and C describe the series resistance, series inductance, shunt conductance, and shunt capacitance per unit length, respectively. The four-port differential line model can be converted to one differential-mode and one common-mode two-port circuit models, as shown in Fig. 3(b) and (c), respectively. The relation between the four- and two-port circuits are also indicated. Note that k is the coupling coefficient of a transformer, and can be calculated by L_m/L. This model will be used for both interconnect analysis and modeling below.

B. Mixed-Mode S-Parameters

Since a four-port differential semicoaxial line is driven by the differential- and common-mode signals, the high-frequency characteristics can be described by the mixed-mode S-parameters. Four 2 $\times$ 2 matrices are included, and referred to as the S-parameters of differential-mode (S_{dd}), differential-to-common-mode (S_{dc}), common-to-differential-mode (S_{cd}), and common-mode (S_{cc}). The measured four-port

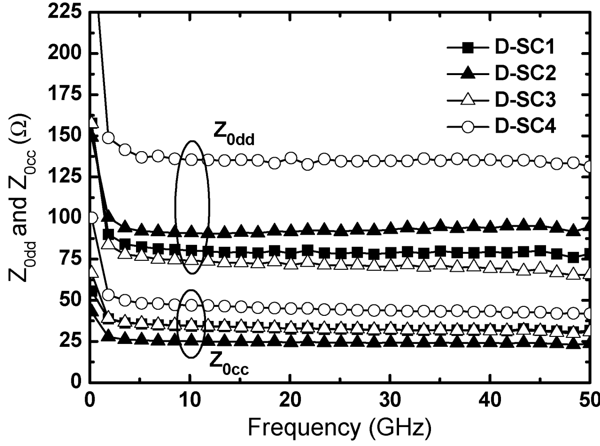

Fig. 4. Differential-mode $Z_0(Z_{0dd})$ and common-mode $Z_0(Z_{0cc})$ for differential semicoaxial lines from [9].

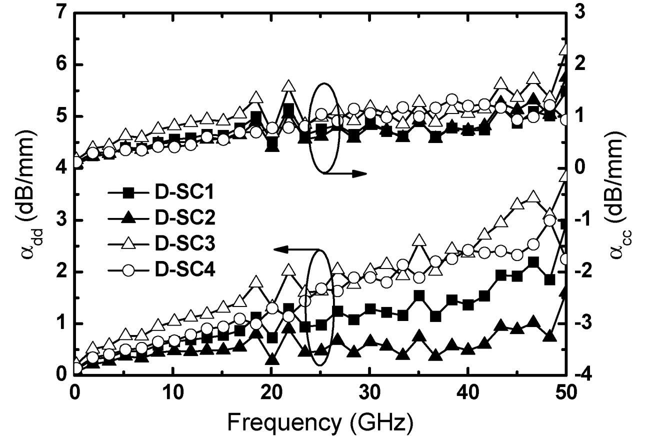

Fig. 5. Differential-mode $\alpha(\alpha_{dd})$ and common-mode $\alpha(\alpha_{cc})$ for differential semicoaxial lines (α_{dd} is from [9]).

S-parameters of differential semicoaxial lines are converted to the mixed-mode S-parameters by the following equation [14]:

$$\begin{bmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{cc11} & S_{cc12} \\ S_{cd21} & S_{dd22} & S_{cc21} & S_{cc22} \end{bmatrix} = [M] \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} [M]^{-1} \quad (1)$$

where

$$[M] = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix}. \quad (2)$$

For a symmetric differential line, as studied here, S_{dc} and S_{cd} are nonexistent, therefore, only S_{dd} and S_{cc} are analyzed.

C. *Mixed-Mode* Z_0 *and* γ

The measured differential-mode $Z_0(Z_{0dd})$ and common-mode $Z_0(Z_{0cc})$ can be obtained from S_{dd} and S_{cc}, respectively [15]. As shown in Fig. 4, Z_{0dd} of each differential semicoaxial line is larger than Z_{0cc}, which can be understood by the Z_0 equations derived from Fig. 3

$$Z_{0dd} = 2\sqrt{\frac{L(1-k)}{C+2C_m}} \quad (3)$$

$$Z_{0cc} = \frac{1}{2}\sqrt{\frac{L}{C}}. \quad (4)$$

As observed from (4), Z_{0cc} is independent of a coupling effect due to the fact that in-phase common-mode signals are not interacting. For a weakly coupled differential line ($k \sim 0$, $C_m \sim 0$), Z_{0dd} and Z_{0cc} should be $\sim 2Z_0$ and $Z_0/2$ ($Z_0 = (L/C)^{0.5}$), respectively. Note that the coupling effect is affected mainly by the metal spacing (S). A small S increases k and C_m, while it also decreases Z_{0dd}. The line D-SC2 follows the relation of $Z_{0dd}/Z_{0cc} \sim 4$ due to a large spacing of 79.5 μm that is employed, while the other three differential semicoaxial lines have Z_{0dd}/Z_{0cc} smaller than 4 resulting from the small S used.

The attenuation constants (α) in both differential-mode (α_{dd}) and common-mode (α_{cc}) are shown in Fig. 5. As can be seen, the losses of all D-SC lines are less than ~3.5 dB/mm at 50 GHz, which can be attributed to the perfectly shielded lossy Si substrate and the wave propagation close to an ideal TEM mode with the semicoaxial structure. For a low-loss and weakly coupled differential line, α_{dd} can be approximated to α_{cc}, as can be derived from the model in Fig. 3 as follows:

$$\alpha_{dd} = \frac{R_{dd}}{2Z_{0dd}} \approx \frac{2R}{2 \times 2\sqrt{L/C}} = \frac{R}{2\sqrt{L/C}} \quad (5)$$

$$\alpha_{cc} = \frac{R_{cc}}{2Z_{0cc}} = \frac{R/2}{2(\sqrt{L/C})/2} = \frac{R}{2\sqrt{L/C}} \quad (6)$$

where R_{dd} and R_{cc} represent the differential- and common-mode resistances, respectively. The line D-SC2 shows a trend of $\alpha_{dd} \sim \alpha_{cc}$ due to a large S that is employed. Since the large coupling effect decreases Z_{0dd}, α_{dd} for the rest of the differential semicoaxial lines are all larger than α_{cc}. In addition, from a comparison between the lines with the same W_s, a larger Z_{0dd} results in a smaller α_{dd}. The trend of α_{dd} in Fig. 5 is consistent with (5). Note that the line D-SC2 shows the lowest α_{dd} of ~1.00 dB/mm at 50 GHz compared with the other geometries, which can be attributed to a wide W_s of 15 μm and a large S of 79.5 μm adopted in the design. A further analysis of different origins of the loss in D-SC lines will be carried out in Section IV.

D. *Slow-Wave Effect*

The slow-wave factor is the ratio of the wave velocity in vacuum (c) to that in dielectric (v). An increased slow-wave factor results in a reduced v, leading to a smaller effective wavelength, which can be very useful for the passive microwave component design such as couplers and dividers [16]. With a large slow-wave factor, the component size, as well as the signal loss can be effectively reduced.

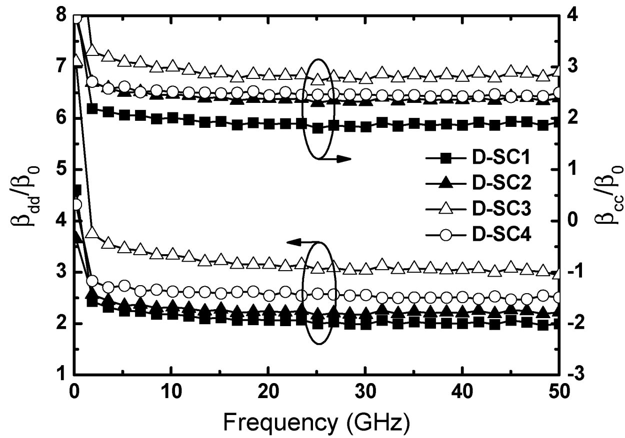

Fig. 6. Differential-mode slow-wave factor (β_{dd}/β_0) and common-mode slow-wave factor (β_{cc}/β_0) for differential semicoaxial lines.

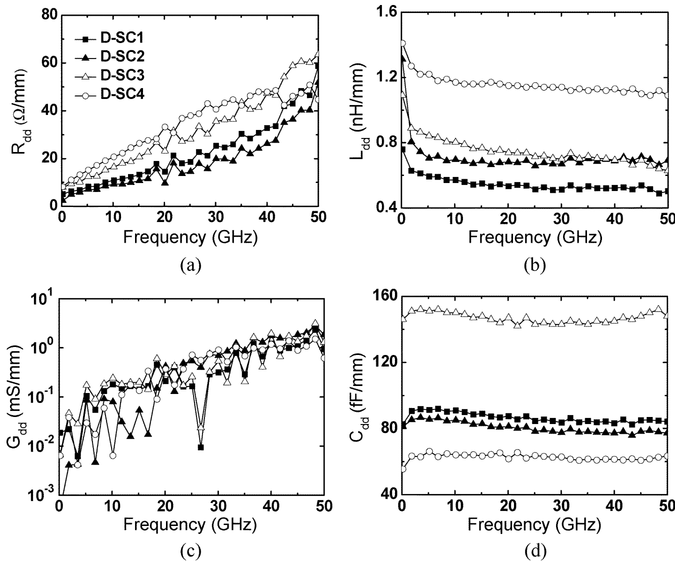

Fig. 7. Differential-mode $RLGC$ for differential semicoaxial lines from [9].

From the phase constant in the vacuum (β_0) and the measured phase constant (β), the obtained slow-wave factor in differential-mode (β_{dd}/β_0) and common-mode (β_{cc}/β_0) are shown in Fig. 6. The observed slow-wave factors are all higher than the square root of the dielectric constant (3.9) of SiO_2 due to the fact that the wave velocity ($v = 1/(LC)^{0.5}$) is reduced by the large L and C. The large L can be mainly attributed to a large current loop area resulting from the semicoaxial structure [17]. The large C is due to the increased ground-plane area and the coupling effect between the signal lines. For example, a high β_{dd}/β_0 of 3.1 is observed in D-SC3. With this structure, the physical size of an interconnect for a certain electrical length can be effectively reduced by a factor of approximately 3 compared to that in vacuum.

E. Mixed-Mode $RLGC$ Components

From Z_0 and γ, the extracted $RLGC$ components for both differential- and common-mode circuit models are illustrated in Figs. 7 and 8, respectively. As shown in Figs. 7(a) and 8(a), R_{dd} and R_{cc} increase with frequency due to the skin effect and

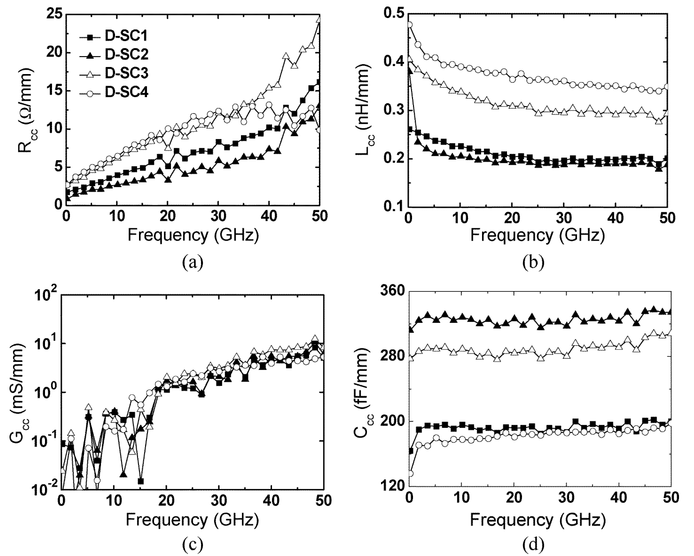

Fig. 8. Common-mode $RLGC$ for differential semicoaxial lines from [9].

proximity effect. In addition, the observed $2R_{cc}$ is higher than $R_{dd}/2$, instead of being equal in an ideal case. This can be attributed to the fact that the common-mode signal currents repel each other at the edges of the signal lines, while the differential-mode both attract each other due to proximity effect. Both effects reduce the current cross section, but the repelled condition results in a relatively smaller area. The increased G_{dd} and G_{cc} with frequency can be attributed to the dielectric conductivity, which is proportional to frequency. From Figs. 7(b) and 8(b), L_{dd} and L_{cc} present an obvious reduction at ~1 GHz because the current loop area is reduced by the skin effect and proximity effect. In addition, the almost frequency-independent C_{dd} and C_{cc} suggest that the dispersion effect of the SiO_2 layer is relatively weak.

F. Coupling Effects

From the differential- and common-mode circuit models, as shown in Fig. 3, the k and C_m can be derived as

$$k = 1 - \frac{L_{dd}}{4L_{cc}} \tag{7}$$

$$C_m = C_{dd} - \frac{C_{cc}}{4}. \tag{8}$$

As depicted in Fig. 9, the measured k and C_m both present a low-frequency dependence. Moreover, both the current and voltage coupling increase when S decreases. For example, a high k and C_m of 0.4 and 75 fF/mm are observed for D-SC3, respectively.

Note that the k and C_m are the critical parameters for the Z_{0dd} design, as described in (3). With a low coupling effect, the Z_0 empirical equations for single lines can be employed directly for differential lines, which provide a simple design approach for differential lines. On the other hand, the required chip area of interconnects designed for low Z_{0dd} can be reduced with high coupling effect. The presence of a high k and C_m in (3) can significantly reduce the required large C and small L. As a result, a low Z_{0dd} differential interconnect can be achieved by small signal linewidth.

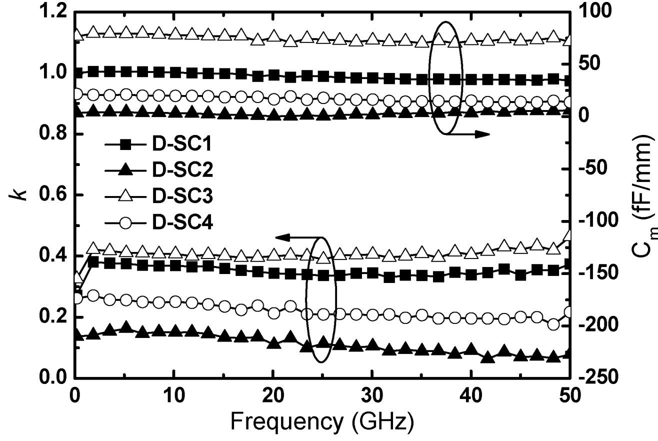

Fig. 9. k and C_m for differential semicoaxial lines.

IV. Modeling of Differential Semicoaxial Lines

Lack of an accurate differential lines model greatly handicaps the differential-type Si-based MMIC design. For CMOS differential lines, an accurate equivalent-circuit model with a wide frequency range is still not available. In this study, a systematic approach is developed to model the differential semicoaxial lines by the lumped-element $RLGC$ circuit model with n sections. Physical-based semiempirical equations are employed, and the model is verified up to 50 GHz. Each identical section of the model has been shown in Fig. 3(a). The sufficient section number n for accurate modeling can be estimated by the following equation:

$$n = 10\frac{f_m \times l}{v} \tag{9}$$

where f_m is the maximum operation frequency, v is the wave velocity, and l is the length of the interconnect. The derivation of (9) is under the assumption that if a section (l/n) of an interconnect is smaller than or equal to $\lambda/10$, a lumped-circuit model can be employed to describe the characteristics accurately. In contrast to the modeling of a single line, additional efforts were made to include the coupling effects in the differential line. R, L, G, and C are calculated first by neglecting one of the signal lines in the differential interconnect, while both signal lines are taken into account for k and C_m. The semirounded structure is simplified by adopting a parallel-plate structure with additional fitting parameters to describe the sidewall effect from the ground plane.

For a grounded interconnect with a lossless substrate, R mainly originates from both the signal and ground metal lines. The ac resistance of the signal line $(R_{\mathrm{AC}-s})$ is dominated by the skin effect resulting from the finite metal width and thickness [15], while the dc part $(R_{\mathrm{DC}-s})$ is based on the simple resistivity equation. On the other hand, the dc resistance of the ground line is negligible due to an overall large metal cross-sectional area, while the ac resistance $(R_{\mathrm{AC}-g})$ can be modeled by the skin effect with an area parameter. Therefore, R can be represented as

$$R = R_{\mathrm{DC}-s} + R_{\mathrm{AC}-s} + R_{\mathrm{AC}-g} \tag{10}$$

TABLE III
Description for Geometrical and Physical Parameters

Symbol	Description
Ws, Wg	Metal width of the signal and bottom ground line
Ts, Tg	Metal thickness of the signal and bottom ground line
Hox	Distance between top and bottom metal layers
S	Spacing between top metal lines
j s, j g	Metal conductivity of the top and bottom layers
i r-real	Real part of the relative dielectric constant of SiO_2
i r-imag	Imaginary part of the relative dielectric constant of SiO_2
i0, μ0	Permittivity and permeability of free space
hs	Skin depth of the signal line

where

$$R_{\mathrm{DC}-s} = (\sigma_s W_s T_s)_g^{-1} \tag{11}$$

$$R_{\mathrm{AC}-s} = (\sigma_s W_s)^{-1}\left(\delta_s\{1-\exp(-T_s/\delta_s)\}\{1+T_s/W_s\}\right)^{-1} \tag{12}$$

$$R_{\mathrm{AC}-g} = A_x\sqrt{f}/\sigma_g. \tag{13}$$

The fitting parameter A_x accounts for the effective ground metal cross section. The descriptions for the geometrical and physical parameters are tabulated in Table III.

The inductance L mainly relates to the current loop area enclosed by the signal and ground lines. Regarding the parallel-plate structure, the concept of geometric-mean-distance (g.m.d.) is utilized to describe the frequency-independent loop inductance $(L_{\mathrm{loop}-s})$ [18]. Since both skin and proximity effects reduce the effective metal width and thickness, an additional frequency-dependent internal inductance $(L_{\mathrm{int}-s})$ is introduced [19]. The total inductance L is a sum of $L_{\mathrm{int}-s}$ and $L_{\mathrm{loop}-s}$, and each component can be written as

$$L_{\mathrm{int}-s} = \frac{\mu_0}{2\pi}\frac{3}{8}\tanh\left(\frac{2\pi\delta_s}{W_s+T_s}\right) \tag{14}$$

$$L_{\mathrm{loop}-s} = \frac{\mu_0}{\pi}\left\{2\ln(r_{sg})-\ln(r_s)-\ln(r_g)+\ln(r_x)\right\} \tag{15}$$

where

$$r_{sg} = 50(2H_{\mathrm{ox}}+T_s+T_g)\times\exp(K_1) \tag{16}$$

$$r_s = 22.31(W_s+T_s) \tag{17}$$

$$r_g = 22.31(W_g+T_g) \tag{18}$$

and where r_{sg} is the g.m.d. between the top and bottom metal layers, K_1 is a geometry-dependent factor, and r_s and r_g are the g.m.d. of the signal and bottom ground lines, respectively. The fitting parameter r_x in (15) is adopted to model the g.m.d. of the sidewall ground plane.

By considering the frequency-dependent dielectric conductivity, the modeled G is proportional to frequency (f) and can be written as

$$G = \varepsilon_0\varepsilon_{r-\mathrm{imag}}2\pi f(W_s/H_{\mathrm{ox}}) + G_x. \tag{19}$$

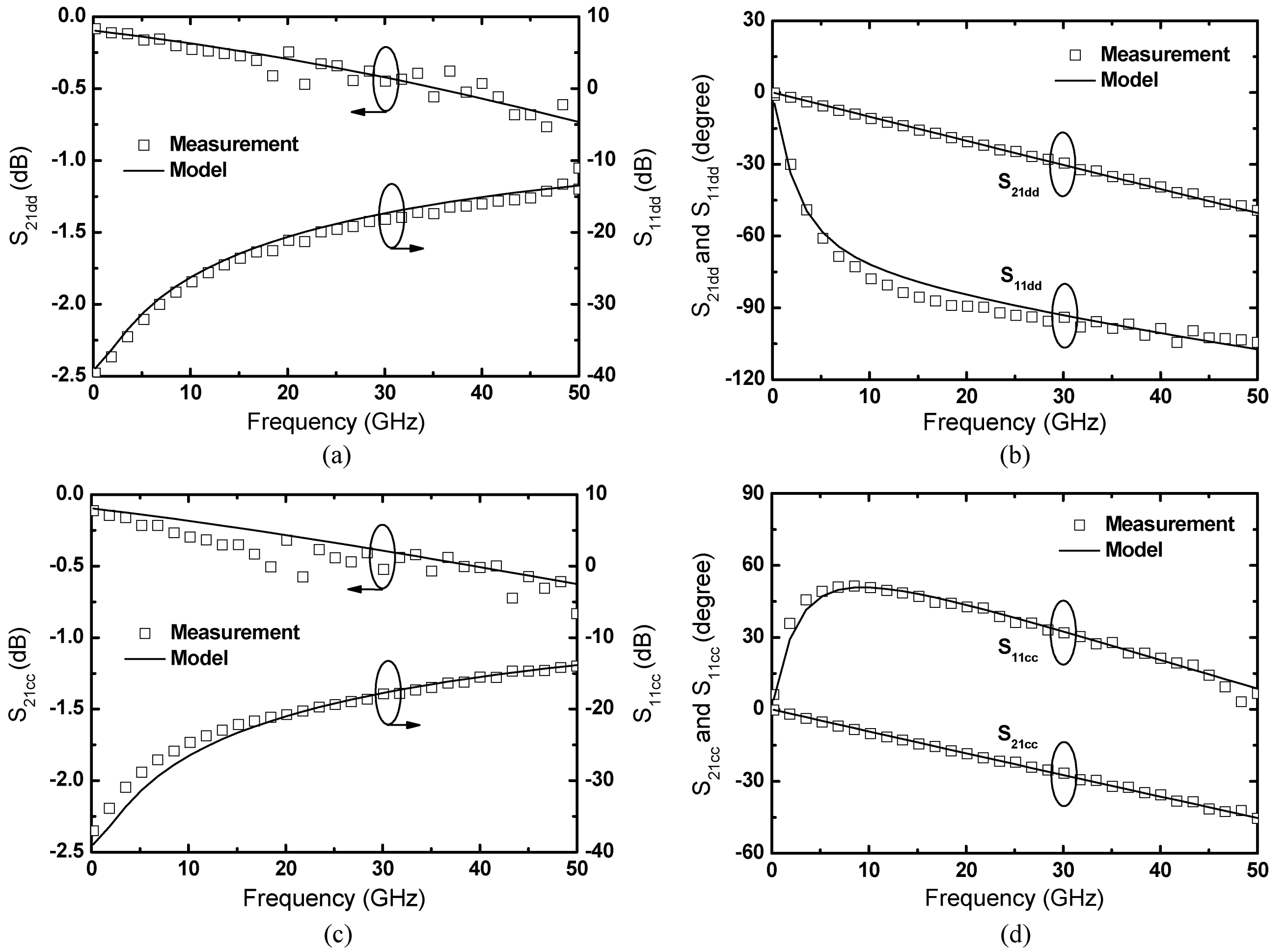

Fig. 10. Measured and modeled mixed-mode S-parameters for line D-SC1. (a) Differential-mode S_{21} and S_{11} in magnitude. (b) Differential-mode S_{21} and S_{11} in phase. (c) Common-mode S_{21} and S_{11} in magnitude. (d) Common-mode S_{21} and S_{11} in phase.

The first term on the right-hand side of (19) accounts for the conductance of the parallel-plate structure, and G_x accounts for the sidewall of the ground plane.

The capacitance C can be calculated by the microstrip line approximation with a geometry-dependent $\epsilon_{r-\text{real}}(\epsilon_{\text{eff}})$ due to the electric field exists in both air and the SiO_2 layer [15]. The additional capacitance introduced by the sidewall is included by C_x. The overall C can be written as

$$C = \varepsilon_0 \varepsilon_{\text{eff}} W_s / H_{\text{ox}} + C_x \tag{20}$$

where

$$\varepsilon_{\text{eff}} = \frac{\varepsilon_{r-\text{real}} + 1}{2} + \frac{\varepsilon_{r-\text{real}} - 1}{2\sqrt{1 + 10 H_{\text{ox}}/W_s}}. \tag{21}$$

As observed from (20), the modeled C is frequency independent, which agrees well with the measured results since the frequency dependence of the dielectric material is negligible in the measured frequency range.

k can be calculated by L_m/L. L_m between two signal lines is simplified to a frequency-independent parameter since the measured results show a low-frequency dependency. Therefore, L_m can be represented as [18]

$$L_m = \frac{\mu_0}{2\pi}\left(\ln(Q + \sqrt{1+Q^2}) - \sqrt{1+Q^{-2}} + Q^{-1}\right) - L_{mx} \tag{22}$$

where

$$Q = l/(W_s + S). \tag{23}$$

The first term on the right-hand side of (22) is derived based on an infinite current loop area, which differs from the confined loop area in the real case. Therefore, a fitting parameter L_{mx} is introduced to compensate for the overestimated mutual inductance.

The C_m consists of a parallel-plate capacitance between two signal lines and a fringing capacitance in the air and SiO_2 layer. The fringing part is represented by a fitting parameter to simplify the model. The modeled C_m is frequency independent.

Based on the developed modeling methodology, an excellent agreement between the measured and modeled mixed-mode S-parameters for differential semicoaxial lines is obtained up to 50 GHz. Fig. 10 shows the results for line D-SC1 as an example. Note that the estimated n is two from (9), while a section number of four was employed here for an improved modeling accuracy.

From the above analysis, the different loss origins in a low-loss D-SC line can be investigated quantitatively. At high frequencies, the dominant differential-mode losses are the conductor loss ($\alpha_{c,dd} = R_{dd}/2Z_{0dd}$) and the dielectric loss ($\alpha_{d,dd} = G_{dd}Z_{0dd}/2$). For line D-SC2 with the lowest $\alpha_{dd}(\alpha_{dd} = \alpha_{c,dd} + \alpha_{d,dd})$ at 50 GHz, the high-frequency conductor loss is mainly due to skin effect. By using (11) and (12), the resistance $R_{\mathrm{DC}-s}$ and $R_{\mathrm{AC}-s}$ are 0.7 and 4.1 Ω/mm, respectively. The calculated $\alpha_{c,dd}$ is 0.46 dB/mm, assuming $R_{\mathrm{AC}-g}$ is negligible. On the other hand, the conductance is 0.6 mS/mm from (19), assuming G_x is negligible, and the estimated $\alpha_{d,dd}$ is 0.47 dB/mm. As a result, the overall calculated loss from both the conductor and dielectric layers is 0.93 dB/mm, which is close to the measured result of 1.00 dB/mm at 50 GHz.

V. CONCLUSION

In this paper, the low-loss differential semicoaxial lines in a standard CMOS process have been investigated in detail. The mixed-mode S-parameters were adopted to characterize the Z_0, α, slow-wave factor, $RLGC$ components, k, and C_m of four-port differential semicoaxial lines. A low α_{dd} of 1.00 dB/mm at 50 GHz was obtained for a differential semicoaxial line with a particular geometry. A large slow-wave factor above 3.1 was observed for differential semicoaxial lines due to the semirounded ground plane. Measured k and C_m showed small frequency dependence. For a differential semicoaxial line with a metal spacing of 2.4 μm, high coupling coefficients of 0.4 and 75 fF/mm were observed. The impacts of coupling effects on Z_{0dd} design were also discussed. In addition, the differential semicoaxial lines were modeled by the lumped-element $RLGC$ circuit model with an excellent accuracy up to 50 GHz.

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Jun-De Jin was born in Taipei, Taiwan, R.O.C., in 1979. He received the M.S. degree in electronics engineering from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., in 2003, and is currently working toward the Ph.D. degree in electronics engineering at National Tsing Hua University.

His research involves the designation of Si-based RF devices and circuits. In the summer of 2004, he was an Intern with the Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, R.O.C., where he studied the characteristics of Si-based interconnects.

Mr. Jin was a recipient of the Gold Medal of the 2001 ELAN Microcontroller Competition, the Silver Medal of the 2002 National Semiconductor Temperature Sensor Competition, and the Bronze Medal of the 2006 TSMC Outstanding Student Research Award.

Shawn S. H. Hsu (M’04) was born in Tainan, Taiwan, R.O.C. He received the B.S. degree in electrical engineering from National Tsing Hua University, Taiwan, R.O.C., in 1992, the M.S. degree in electrical engineering and computer science from The University of Michigan at Ann Arbor, in 1997, and the Ph.D. degree from National Chiao Tung University, Taiwan, R.O.C., in 2003.

From 1992 to 1994, he was a lieutenant in the R.O.C. Army. From 1994 to 1995, he was a Research Assistant with National Chiao Tung University. In

1997, he joined the III–V Integrated Devices and Circuits Group, National Chiao Tung University. He is currently an Assistant Professor with the Department of Electrical Engineering, National Tsing Hua University. His current research interests include the analytical and empirical large-signal and noise modeling of Si/III-V based devices for RFIC/MMIC design applications, the implementation and development of various measurement techniques to extract parameters for equivalent-circuit models, and the design of MMICs and RFICs using Si/III-V based devices for low-noise, high-linearity, and high-efficiency system-on-chip (SOC) applications.

Ming-Ta Yang (S'93–A'06) was born in Tainan, Taiwan, R.O.C., in 1966. He received the B.S and M.S. degrees in physics and applied physics from Chung-Yuan University, Chung -Li, Taiwan, R.O.C., in 1989 and 1992, and the Ph.D. degree in electrical engineering from National Central University, Chung-Li, Taiwan, R.O.C., in 1995. His doctoral dissertation was focused on the characterization and model of AlGaAs/InGaAs doped-channel heterostructure field-effect transistors (FETs) and its application in MMICs.

During the 1989 academic year, he joined the Department of Physics, Chung-Yuan University, as a member of the faculty. In 1995, he joined Mosel Vitelic Inc., Hsin-Chu, Taiwan, R.O.C., where he was involved with very large scale integration (VLSI) advanced technology development. In 1998, he then joined the Taiwan Semiconductor Manufacture Company Ltd. (TSMC), Hsinchu, Taiwan, R.O.C., where he set up the High-Frequency Characterization Laboratory and organized a team to response for the development of characterization and SPICE model both in mixed-signal and RF applications. His current research interests include the development of advanced high-frequency characterization and modeling of devices both in RF CMOS and high-speed SiGe HBT BiCMOS technologies. He is currently the Manager of the Device (MOS, HBT and passive) Modeling, and Characterization Service Team, where he is responsible for mixed-signal/RF device modeling. He has authored or coauthored over 30 technical papers in international journals and conferences in the area of RF device characterization and modeling covering the fields of III–V AlGaAs/InGaAs HEMTs, Si/SiGe BiCMOS, and mostly in the RF CMOS.

Dr. Yang served on the Advisory Workshop Committees of Compact Modeling for RF/Microwave Applications (CMRF) (2004–2006) and as a committee member on "Device and Modeling" of the SiRF in 2007.

Sally Liu received the B.S. and M.S. degrees in physics and applied physics from National Tsing-Hua University, Hsinchu Taiwan, R.O.C., in in 1972 and 1974, respectively, and the Ph.D. degree in electrical engineering and computer science from University of California at Berkeley, in 1981.

Since 2004, she has been Director of the Advanced Technology Modeling Division, Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, R.O.C. Prior to this, she spent 15 years with AT&T Bell Laboratories, six years with Conexant/Rockwell Semiconductors, and two years with RFIC. She has been engaged in the research and development of device modeling and simulation, circuit simulation and optimization, statistical modeling and design centering, circuit verification, intellectual property (IP) characterization, and electrical design automation (EDA) framework.