國 立 清 華 大 學
博 士 論 文

應用於無線-有線通訊之微波 CMOS 積體放大器

Microwave CMOS Integrated Amplifiers for Wireless/Wireline Communications

系 所 別：電機工程學系電子工程研究所

姓　　名：金俊德　(Jun-De Jin)

學　　號：**929003**

指導教授：徐碩鴻　博士　(Dr. Shuo-Hung Hsu)

中 華 民 國 九 十 七 年 十 二 月

Microwave CMOS Integrated Amplifiers for Wireless/Wireline Communications

by

Jun-De Jin

Submitted to the Electronics Engineering in Partial Fulfillment of

the Requirements for the Degree of

Doctor of Philosophy in Electronics Engineering

at the

National Tsing Hua University

December 2008

Advisor

Dr. Shuo-Hung Hsu

Abstract

This study proposed new circuit design techniques to achieve high-performance CMOS integrated amplifiers for wireless/line communications at microwave frequencies. The design concepts were demonstrated by one narrowband and one broadband amplifiers, which were both realized in the standard 0.18-μm RF CMOS technology. The measured results presented superior performances compared with other published works using a similar or even more advanced CMOS technology.

The designed narrowband amplifier is a 24-GHz balanced amplifier (BA) with a gain up to 45 dB. An effective technique, π–type parallel resonance (PPR), was proposed to boost the high frequency gain of a MOSFET by resonating out the inherent capacitances. The miniaturized lumped-element coupler in the circuit occupies a chip area of only ~ 2 % compared to that of the conventional transmission-line coupler. The BA consumes 123 mW from a supply voltage of 1 V. The proposed CMOS BA presents the highest gain of 45.0 dB with a chip area of 0.97 × 0.63 mm^2 (core area: 0.78 × 0.43 mm^2) among the published narrowband amplifiers with similar technologies and operation frequencies.

The designed broadband amplifier is a 40-Gb/s transimpedance amplifier (TIA). From the measured S-parameters, a transimpedance gain of 51 dBΩ and a 3-dB bandwidth up to 30.5 GHz were observed. A gain-bandwidth product (GBW) enhancement technique, π-type inductor peaking (PIP), is proposed to achieve a bandwidth enhancement ratio (BWER) of 3.31. In addition, the PIP topology used at the input stage decreases the noise current as the operation frequency increases. Under a 1.8 V supply voltage, the TIA consumes 60.1 mW with a chip area of 1.17 × 0.46 mm^2. The proposed CMOS TIA presents a GBW per DC power figure-of-merit (GBP/P_{dc}) of 180.1 GHzΩ/mW.

摘要

本文針對微波頻段的無線-有線通訊系統提出了二個創新的技巧用於增加 CMOS 積體電路放大器的效能。我們將這二個方法分別展示在一個窄頻放大器和一個寬頻放大器中，且這第二個放大器都使用了標準的 0.18-μm RF CMOS 製程。與使用相同或更先進製程的文獻相比，這二個放大器的效能皆優於或可與其相提並論。

所設計的窄頻放大器為操作在 24 GHz、增益為 45 dB 的平衡式放大器 (Balanced amplifier, BA)。此放大器使用了本文所提出的窄頻電路技術：π 型並聯共振器(π-type parallel resonance, PPR)。藉由共振掉電晶體天生的寄生電容，PPR 可有效的增加電晶體的高頻增益。在耦合器的設計方面，我們使用了微小式的集總元件耦合器因為此面積只有傳統的傳輸線耦合器的 2 %。所設計的 BA 特性為：操作電壓 1 V、消耗功率 123 mW、增益 45 dB、晶片面積 0.97 × 0.63 mm^2、主要電路面積 0.78 × 0.43 mm^2。跟其它使用相同製程和操作頻率的窄頻放大器所比，此放大器的增益為最高。

所設計的寬頻放大器為 40-Gb/s 的轉阻放大器(Transimpedance amplifier, TIA)。此放大器使用了本文所提出的寬頻電路技巧：π 型電感式 peaking (π-type inductor peaking, PIP)。對一個共源級放大器而言，PIP 可增加頻寬達 3.31 倍。另外，PIP 用於輸入級也可使得雜訊電流隨著頻率增加而減少。所設計的 TIA 特性為：操作電壓 1.8 V、消耗功率 60.1 mW、轉阻增益 51 dBΩ、頻寬 30.5 GHz、晶片面積 1.17 × 0.46 mm^2、增益頻寬積除以直流功率 180.1 GHzΩ/mW。

Acknowledgements

首先感謝求學過程中啟發和提攜我的長輩們：東南工專的洪鴻文老師和郎宏德老師、清華大學的呂助增老師和徐碩鴻老師、和台積電的楊明達經理。還有一位扮演重要關鍵的長輩，現任嘉義大學的羅光耀老師。

我的實驗室生涯可以追溯到我在五專時期的第五年。當時一同渡過辛苦但有趣的日子有小明、吳元吉、歷蘇、和周蘇豪等。常常為了買零件而一起穿梭在光華商場、寧夏商場、景美等地。晚上八點以後回家是基本的，有時因為無法完成實驗而要徹夜待在實驗室。第一次體驗到實驗室的苦日子但後來的成果相對之下也就更甜美了。

後來升學到了崑山科大。第一次離開台北到了台南，有陳其倫常常帶我趴趴走體驗台南這個古都。學業上的伙伴則有嘉健、育達等。

碩士班來到了清華大學的固態電子實驗室。由於這是一個大的實驗室，所以有許多學長學姐可以學習。另外，跟同一屆的志維學英文、學經濟、學生活哲學等。從葉彥顯身上學習到了做研究的方法與態度，這對我在讀博士期間的研究態度有很大的影響。

博士班選擇了剛回國教書的徐碩鴻老師。實驗室的設備可說從零開始。不過還好研究上還是有智元、于軒、和歷年的學弟等可以互相討論與尋找儀器。

最後，感謝我的家人一路上的支持和陪伴。尤其是在一起十年今年剛嫁給我的太太張加。十年的光陰中，百分之九十的時間我們都是分隔兩地。真的非常感謝妳的支持與體諒。

Contents

List of Figures

List of Tables

Chapter I: Introduction

The dramatically increased demand on the data capacity has push the operation frequency of the wireless system toward 24- and 60-GHz and the data rate of the wireline system toward 40- and 100-Gb/s. Traditionally, the circuit blocks of these systems were built by using III-V [1]-[5] or SiGe [6]-[10] technologies due to the superior transistor performances in the microwave frequency range. The continuous scaling also makes CMOS technology an excellent candidate for microwave applications, which owns the advantages of high integration level, high yield, low power consumption, and low cost compared with other technologies. However, the ultimate limitations for the operation frequency of MOSFETs (unity current gain cut-off frequency f_T and maximum oscillation frequency f_{max}) and the CMOS-based circuits are still the inherent capacitances of the transistors, which include gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, and drain-source capacitance C_{ds} [11]. The relations between f_T, f_{max} and the parasitic capacitances can be expressed as [12]:

$$f_T = g_m / \left(2\pi\left(C_{gs} + C_{gd}\right)\right) \tag{1.1}$$

$$f_{max} \propto \sqrt{f_T / C_{gd}} \tag{1.2}$$

where g_m is the transonductance of MOSFET.

To improve the transistor speed, several circuit techniques have been reported for narrowband and broadband applications. For narrowband circuits, the basic idea is using the inductor to resonate out the parasitic capacitances in parallel [13]-[16]. The number of the *LC* resonators is usually one or two. In this study, the π-type parallel resonance

(PPR) is proposed which employs three resonators to further enhance the frequency response [17]-[18].

To demonstrate the proposed PPR, a 24-GHz 45-dB gain CMOS balanced amplifier (BA) with a noise figure (NF) of 10.8 dB was designed and implanted by 0.18-μm CMOS technology [17]. The proposed high-gain BA can be employed as a gain block for the post-stage amplification to further increase the signal level, as shown in Fig. 1.1. In this case, its contribution to the total noise figure is not significant if a low-noise amplifier (LNA) is used as the previous stage. Linearity is also an important consideration, and there is typically a trade-off between linearity and gain. For the high-gain design here, a relatively lower input 1-dB gain compression point $P_{1dB,in}$ is expected. This amplifier may find suitable applications in a communication system where the received signal level is low at the front-end, thus the low $P_{1dB,in}$ point is not a major concern. With the high-gain amplifier used, the overall signal level can be boosted substantially to relax the requirement for other stages in the system. For example, a mixer with a small conversion gain or even a passive type can be used to maintain an overall signal linearity.

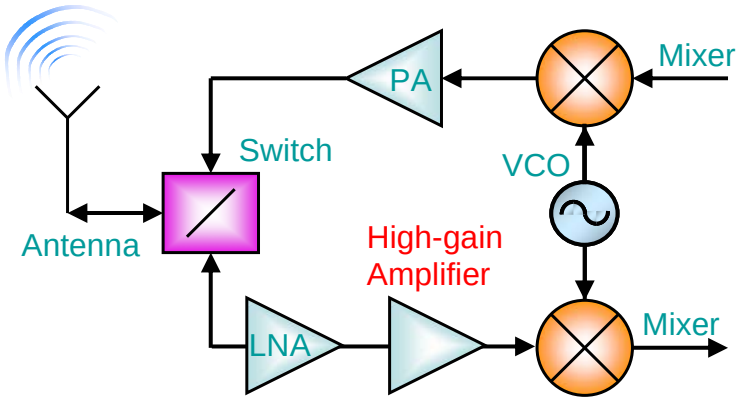


Fig. 1.1. Block diagram of a typical wireless communication system with a high-gain amplifier inserted between the LNA and mixer..

For broadband circuits, there are many strategies such as f_T doubler [19], negative Miller capacitance [19]-[20], negative impedance converter [19], distributed amplifier (DA) [21]-[25], and inductive peaking technique [26]-[34], as shown in Fig. 1.2. The first three techniques can only be realized in a differential configuration, which often limits their applications. The DA configuration is a popular technique but the power consumption and chip area are usually large. This is because each gain stage is connected in parallel instead of cascaded together. Another popular choice is the inductive peaking technique. The basic idea is that the inductor introduces a zero to cancel the original *RC* pole to extend the circuit bandwidth. Here, an effective technique of π-type inductor peaking (PPR) is proposed which presents a bandwidth enhancement ratio (BWER) up to 3.31 [29]-[30].

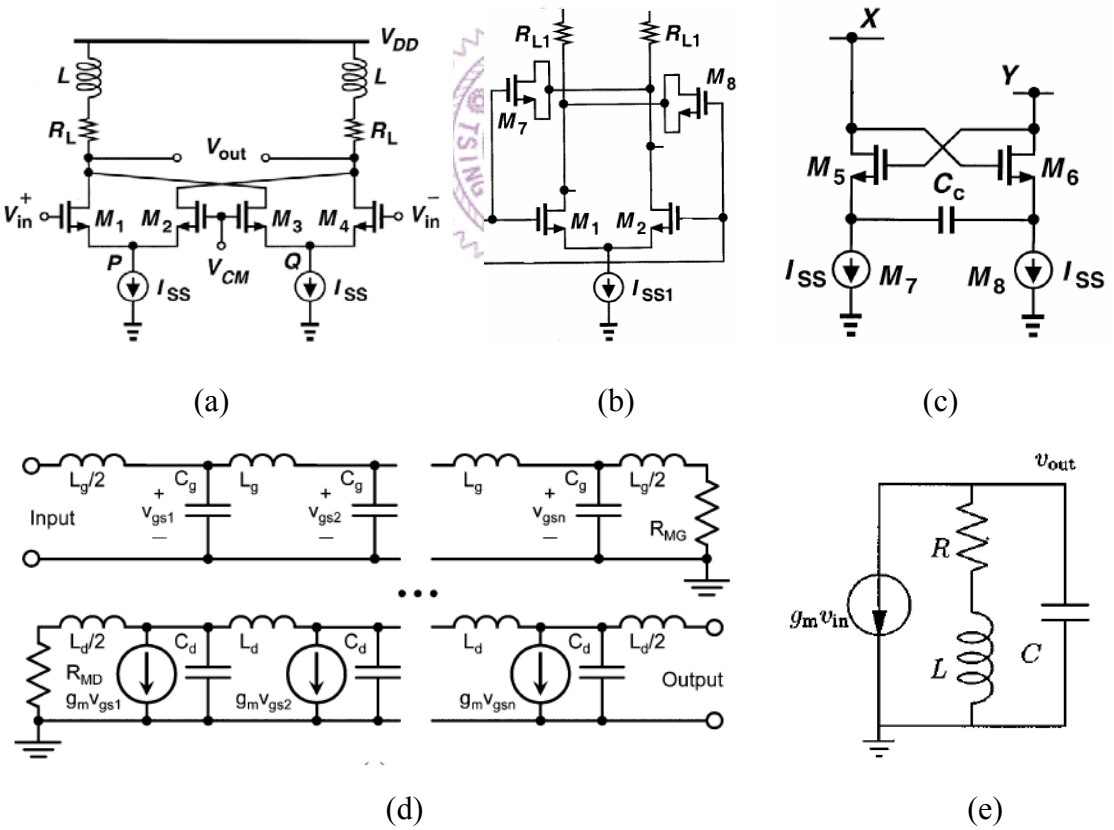


Fig. 1.2. Reported gain-bandwidth product (GBW) enhancement techniques for broadband circuits: (a) f_T doubler, (b) negative Miller capacitance, (c) negative impedance converter, (d) distributed amplifier, and (e) inductive peaking technique.

For the wireline communication system, transimpedance amplifier (TIA) plays an important role since it is the first gain stage of the receiver chain, as shown in Fig. 1.3. A 40-Gb/s TIA is realized in a 0.18-μm CMOS technology to demonstrate the proposed PIP technique [29]-[30]. In addition to the bandwidth enhancement, TIA designed with PIP presents a trend of decreasing input-referred noise current as the operation frequency increases in the desired bandwidth.

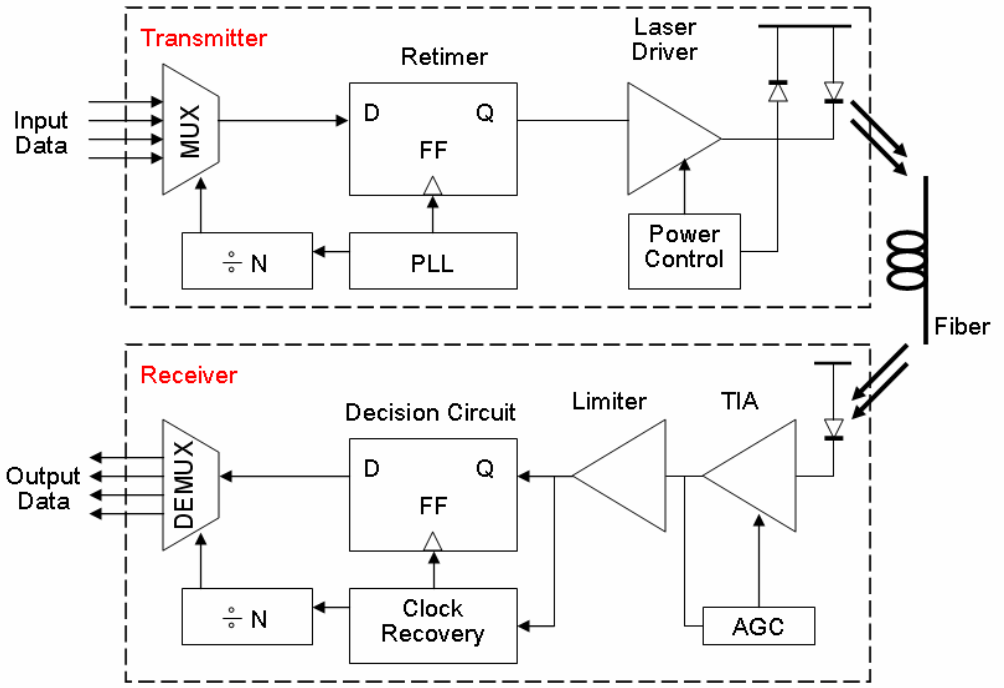


Fig. 1.3. Block diagram of the wireline communication system.

1.1 Overview of Thesis

The remaining chapters in this thesis include the analysis and design method of PPR and PIP in Chapter II and III, respectively. The design details, simulation results, and measurement results of the 24-GHz BA using PPR technique are presented in Chapter IV, and those of the 40-Gb/s TIA using PIP technique are described in Chapter V. Finally, Chapter VI concludes this thesis.

Chapter II: Performance Boosting Techniques for Narrowband Amplifiers

To improve the transistor speed for narrowband amplifiers, the basic idea is using inductors to resonate out the parasitic capacitances in parallel [13]-[16]. The number of the *LC* resonators is usually one or two. Here, the π-type parallel resonance (PPR) is proposed which employs three resonators to have a further enhanced frequency response [17]-[18].

2.1 π-type Parallel Resonance (PPR)

From the modeling point of view, a detailed equivalent circuit model of a RF MOSFET can be represented as shown in Fig. 2.1 [35]-[36]. The core transistor is a BSIM model for logic MOSFET, and the resistors (R_{gm}, R_{dm}, and R_{sm}) and capacitors (C_{gsm}, C_{gdm}, and C_{dsm}) account for the parasitics from the external metal routing. The junction diode D_{dbf} is the area and field-edge sidewall diode from drain to bulk, and D_{dbg} is the gate-edge. In addition, D_{sbf} and D_{sbg} are for those from source to bulk. The resistors (R_{dbm}, R_{sbm}, and R_{bm}) and capacitors (C_{dbm}, C_{sbm}, and C_{bm}) account for the effects from Si substrate. For a common-source (CS) amplifier, a simplified equivalent circuit model can be used, as shown in Fig. 2.2, where the bulk and source are connected to the ground. Based on this simplified circuit model, the RF performance of a MOSFET is ultimately limited by the inherent capacitances including gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, and drain-source capacitance C_{ds}. A simple yet effective approach, PPR, is proposed here to improve the device frequency response [17]-[18]. By adopting inductors in parallel with the intrinsic capacitances, the parallelly resonated *LC* networks become an open circuit at the desired operation frequency f_o. As

a consequence, the capacitance limited high frequency response of the MOSFET can be improved significantly.

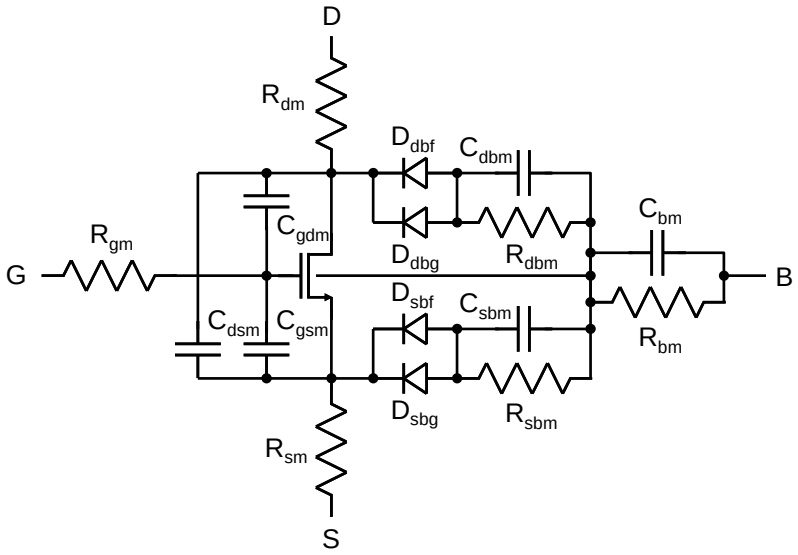


Fig. 2.1. Detailed equivalent circuit model of a RF MOSFET.

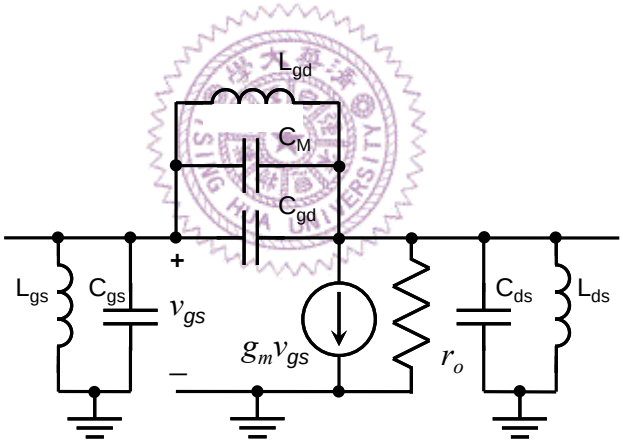


Fig. 2.2. Simplified small-signal equivalent circuit model of a MOSFET with π-type parallel resonance (PPR).

As shown in Fig. 2.2, the PPR inductors are the gate-source inductor L_{gs}, gate-drain inductor L_{gd}, and drain-source inductor L_{ds}, and C_M is an intentional Miller capacitor. Using the simple resonant equation for a parallel LC network, the inductances can be determined by:

$$L_{gs} = 1/\left(f_o^2 C_{gs}\right) \tag{2.1}$$

$$L_{ds} = 1/\left(f_o^2 C_{ds}\right) \tag{2.2}$$

$$L_{gd} = 1/\left(f_o^2 \left(C_{gd} + C_M\right)\right) \tag{2.3}$$

With the inductors properly designed, the devices can achieve a maximum voltage gain A_0 of $g_m r_o$ at f_o, where g_m and r_o are the transconductance and the output resistance of the MOSFET, respectively. It has been reported that using L_{gd} as the neutralization technique is impractical because a large inductance is required [16]. In this design, an additional capacitor C_M is inserted between the gate and the drain to lower the required L_{gd}. At the resonant frequency f_o, the L and C cancel each other thus only a parallel resistor R_p exists between the two terminals, where R_p is mainly originated from the parasitic series resistance of an on-chip spiral inductor. These parasitic resistances, especially the one resulting from L_{gd}, can severely degrade the gain A_0. A simple method to reduce the undesired resistance in the LC resonant circuit is to use a smaller inductor by increasing the capacitance. With a capacitor C_M connected between the gate and the drain intentionally, the required L_{gd} to resonate at f_o can be effectively reduced.

2.2 Effectiveness of PPR

Fig. 2.3 compares different cases to illustrate the merit of using the proposed PPR technique. For a CS stage biased at V_{GS}= V_{DS}= 1V, the simulated power gain S_{21} is 4.2 dB at 24 GHz. In addition, the maximum available gain G_{ma} and the unilateral power gain U are also calculated, which can be written as [37]:

$$G_{ma} = \left|\frac{S_{21}}{S_{12}}\right|\left(k \pm \sqrt{k^2 - 1}\right) \tag{2.4}$$

$$U = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2k\left|\frac{S_{21}}{S_{12}}\right| - 2\,\mathrm{Re}\left(\frac{S_{21}}{S_{12}}\right)} \tag{2.5}$$

where

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}||S_{21}|} \tag{2.6}$$

At 24 GHz, the simulated G_{ma} and U are 9.5 dB and 10.0 dB, respectively. By employing three ideal PPR inductors, S_{21} can be improved up to 7.9 dB. The boosted performance is only 1.6 dB and 2.1 dB smaller than G_{ma} and U, respectively. With the real inductors and C_M in the CMOS process, S_{21} is enhanced to 5.9 dB.

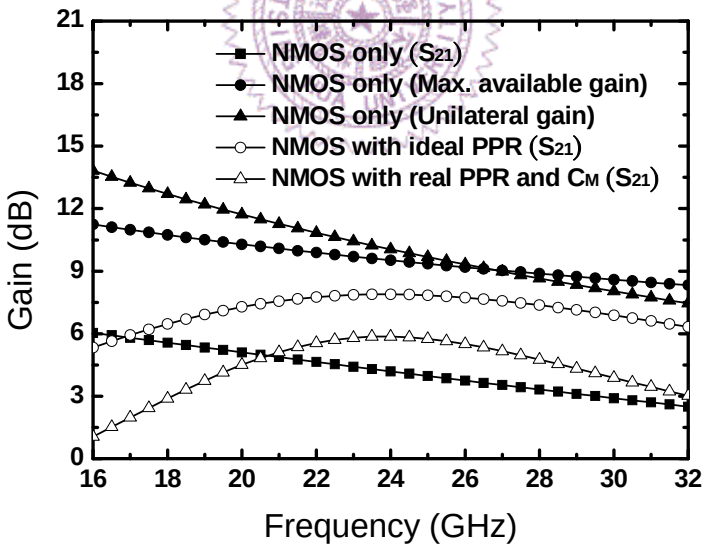


Fig. 2.3. Simulated power gain of a common-source (CS) stage without and with ideal/real PPR inductors.

2.3 Noise Analysis

At the resonant frequency, the circuit in Fig. 2.2 can be simplified as a

voltage-controlled current source and r_o. In this case, the only noise source is the drain thermal noise current. The derived input-referred noise voltage and current can be written as:

$$\overline{v_{n,in}^2} = 4kT\gamma / g_m \tag{2.7}$$

$$\overline{i_{n,in}^2} = 0 \tag{2.8}$$

where γ is the noise factor of the drain thermal noise. Therefore, the noise figure (NF) can be written as:

$$NF = 1 + \frac{\left(\sqrt{\overline{i_{n,in}^2}} + \sqrt{\overline{v_{n,in}^2}} Y_s\right)^2}{4kT / R_s} = 1 + \frac{\gamma}{g_m R_s} \tag{2.9}$$

where R_s and Y_s are the resistance and admittance of the source impedance, respectively. For a typical γ value of 1, a source impedance of 50 Ω, and a g_m of 30 mS, a low NF of 2.2 dB can be expected. However, the parasitic effects of NMOS, PPR inductors, and C_M introduce more noise sources. A higher simulated NF of 4.9 dB is obtained at 24 GHz for the case of NMOS with real PPR and C_M.

2.4 Summary

With three external inductors, the proposed PPR technique can increase the gain of the MOS transistors and circuits effectively. This promising technique can be used in many building blocks of narrowband communication systems to boost the performances. A high-gain 24-GHz balanced amplifier employs the PPR technique will be demonstrated in Chapter IV.

Chapter III: GBW Enhancement Techniques for Broadband Amplifiers

For the small-signal equivalent circuit model of a cascaded CS amplifier, as shown in Fig. 3.1, we can assume that the 3-dB bandwidth of each stage is determined by the drain resistance R_d, equivalent drain capacitance C_d, and equivalent gate capacitance C_g of the next stage. The ratio of C_g to C_d can be determined from the BSIM 3 model provided by the foundry for a more practical estimation. The extracted C_g/C_d is frequency dependent, varying between 2.5 and 3.5 (0.5 ~ 60 GHz). Note that the f_T of 0.18-μm MOSFEETs is ~ 60 GHz (estimated from the foundry provided transistor model). To simplify the circuit analysis, C_g/C_d is set to be 3 here. Based on this small-signal circuit model, three different inductor peaking techniques and the proposed π-type inductor peaking technique will be compared in the following sections.

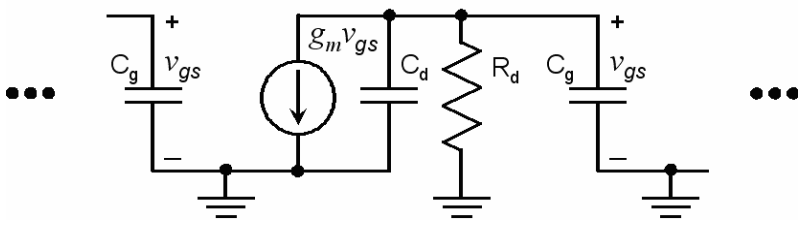


Fig. 3.1. Small-signal equivalent circuit model of a cascaded CS amplifier.

3.1 Shunt Peaking

The most straightforward bandwidth enhancement technique is probably shunt peaking [26]. By placing an inductor L_d in series with R_d, C_d and C_g of the next stage can be canceled out by a shunt LC resonance. A different explanation is that the peaking inductor introduces a zero to extend the circuit bandwidth. Based on the transimpedance transfer function, the design equation for L_d can be derived and written as:

$$L_d = m_d R_d^2 \left(C_d + C_g \right)$$

(3.1)

With an m_d of 0.71, the maximum achievable BWER is 1.85 with a gain peaking of 1.5 dB, as shown in Fig. 3.2, curve *b*. Note that curve *a* shows the normalized frequency response of this circuit without any bandwidth enhancement method applied.

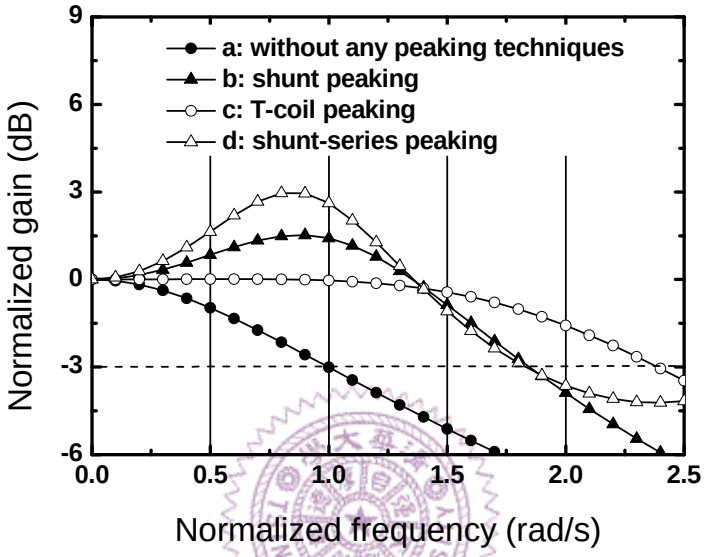


Fig. 3.2. Bandwidth improvement by three previously published wideband techniques. [26]-[28]

3.2 T-coil Peaking

A more effective technique is the T-coil peaking which utilizes one transformer and one capacitor [27]. The primary coil L_{dp} is connected between the drain node and C_g, and the secondary coil L_{ds} is between R_d and C_g. In addition, the bridge capacitor C_B is connected between drain node and R_d. Without considering C_d, the design equations for the transformer and capacitor can be written as:

$$L_{dp} = L_{ds} = \frac{C_g R_d^2}{4} \left(1 + \frac{1}{4\zeta^2} \right)$$

(3.2)

$$k = \frac{4\zeta^2 - 1}{4\zeta^2 + 1} \tag{3.3}$$

$$C_B = \frac{C_g}{16\zeta^2} \tag{3.4}$$

For a flat group delay response, a ζ of $\sqrt{3}/2$ was designed which results in a BWER of 2.82 if C_d is neglected. Note that the BWER obtained in Fig. 3.2, curve *c* is 2.40 since C_d is taken into account for a fair comparison.

3.3 Shunt-Series Peaking

The third technique is shunt-series peaking which employs two inductors, one inductor L_d is in series with R_d and the other inductor L_s is with C_g [28]. The design equation for both inductors can be written as:

$$L_d = \frac{L_s}{2} = \frac{R_d^2\left(C_d + C_g\right)}{4} \tag{3.5}$$

The original circuit analysis presented in [28] shows a BWER of 3.46 with a gain peaking of 1.8 dB based on the assumption that the ratio of C_g to C_d is one. However, the value is reduced to 1.83 when a more practical ratio of three is used, as shown in Fig. 3.2, curve *d*.

3.4 π-type Inductor Peaking (PIP)

Here, a more effective bandwidth extension technique is proposed. On the basis of including the drain capacitance C_d, and with a C_g/C_d ratio of 3, an improved BWER up to 3.31 can be obtained. The details will be discussed in the following sections.

3.4.1 Design Concept of PIP

Fig. 3.3 shows the small-signal equivalent circuit model of a cascaded CS stage

including the PIP inductors (L_{d1}, L_{s1}, and L_{d2}), where R_{d1} and R_{d2} are the drain bias resistors. The progressive bandwidth improvement by adding each peaking inductor is described as follows.

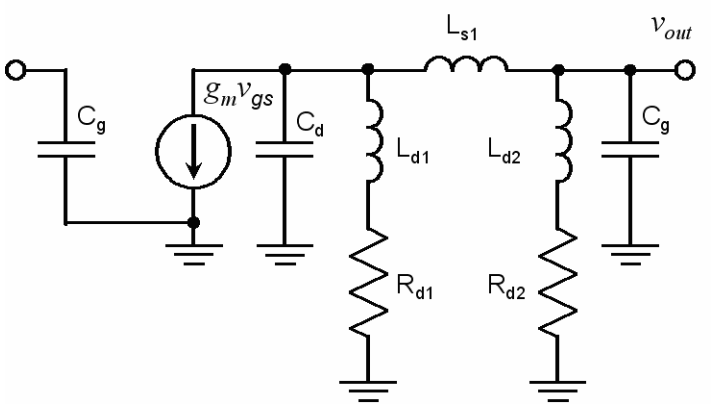


Fig. 3.3. The equivalent circuit model of one gain stage with the π–type inductor peaking (PIP) technique.

Without the PIP inductors, the drain current $g_m v_{gs}$ flows into C_d, C_g, R_{d1}, and R_{d2}, and generates the output voltage v_{out}. In this case, the 3-dB bandwidth ω_0 is limited by the resistive and capacitive loads. By inserting L_{d2} in series with R_{d2}, the bandwidth is increased by a parallel resonance with C_d and C_g. An alternative explanation is that the inductor delays the transient current into R_{d2} and forces more current to flow into the loading capacitor, which improves the speed of the output transient signal and results in an increased circuit bandwidth. If L_{s1} is also employed, the bandwidth can be further enhanced by a series resonance with C_g at higher frequencies, which forces more drain current to flow through L_{s1} and reach the output terminal. In time domain, the transient current charges the two capacitors separated by L_{s1} at different times. As a result, the charging time is reduced leading to an improved bandwidth. Finally, by introducing one more inductor L_{d1}, C_d and C_g can be resonated in parallel with L_{d1} at even higher frequencies to obtain a further enhanced bandwidth. Based on the circuit shown in Fig. 3.3, Fig. 3.4 shows the frequency response of the above four conditions, where ω_0 and the DC gain are both normalized. The gradually improved bandwidth can be observed

as adding the three peaking inductors step by step.

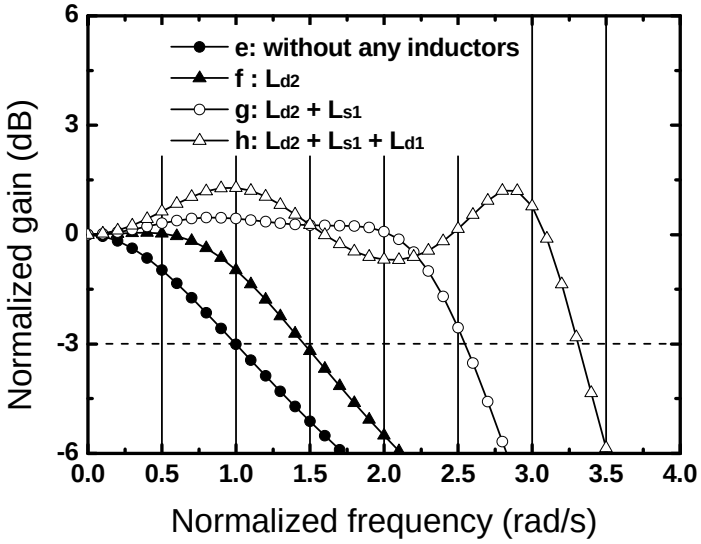


Fig. 3.4. Comparison of the bandwidth enhancement results using PIP technique under different numbers of peaking inductors, where $C_g = 3C_d$ and $R_{d1} = R_{d2}$.

3.4.2 Transfer Function of PIP

To obtain a more comprehensive understanding of the frequency response, the transimpedance transfer function $Z_{PIP}(s)$ of the circuit in Fig. 3.3 is derived as:

$$Z_{PIP}(s) = \frac{v_{out}}{-g_m v_{gs}} = R_{d1}R_{d2}\frac{1 + s\left(\frac{L_{d1}}{R_{d1}} + \frac{L_{d2}}{R_{d2}}\right) + s^2\frac{L_{d1}}{R_{d1}}\frac{L_{d2}}{R_{d2}}}{D_0 + sD_1 + s^2D_2 + s^3D_3 + s^4D_4 + s^5D_5} \tag{3.6}$$

where

$$\begin{aligned}
D_0 &= R_{d1} + R_{d2} \\
D_1 &= L_{d1} + L_{d2} + L_{s1} + R_{d1}R_{d2}\left(C_d + C_g\right) \\
D_2 &= \left(C_d + C_g\right)\left(R_{d1}L_{d2} + R_{d2}L_{d1}\right) + R_{d1}L_{s1}C_d + R_{d2}L_{s1}C_g \\
D_3 &= L_{d1}C_d\left(L_{d2} + L_{s1}\right) + L_{d2}C_g\left(L_{d1} + L_{s1}\right) + R_{d1}R_{d2}L_{s1}C_dC_g \\
D_4 &= L_{s1}C_dC_g\left(R_{d1}L_{d2} + R_{d2}L_{d1}\right) \\
D_5 &= L_{d1}L_{d2}L_{s1}C_dC_g
\end{aligned} \tag{3.7}$$

As can be clearly observed, two zeros R_{d1}/L_{d1} and R_{d2}/L_{d2} existed in $Z_{PIP}(s)$. By an appropriate design, the zeros can be employed to enhance the bandwidth. The required inductances for bandwidth improvement are determined one by one analytically as follows.

To derive L_{d2}, the effects of L_{d1} and L_{s1} are first neglected by setting $L_{d1}= L_{s1}= 0$ in (3.6). Normalized by the DC impedance $R_{d1}//R_{d2}$, the transfer function $z_{Ld2}(s)$ becomes:

$$z_{Ld2}(s)=\frac{1+sL_{d2}/R_{d2}}{1+s\dfrac{\left(L_{d2}+R_{d1}R_{d2}\left(C_d+C_g\right)\right)}{R_{d1}+R_{d2}}+s^2\dfrac{R_{d1}L_{d2}\left(C_d+C_g\right)}{R_{d1}+R_{d2}}} \tag{3.8}$$

The equation indicates that the numerator includes a zero $\omega_{z1}= R_{d2}/L_{d2}$ and the denominator contains a pair of complex conjugate poles $\omega_{Ld2,p1}$ and $\omega_{Ld2,p2}$, which can be written as:

$$\begin{aligned} &s^2+s\left(\frac{1}{R_{d1}\left(C_d+C_g\right)}+\frac{R_{d2}}{L_{d2}}\right)+\frac{R_{d1}+R_{d2}}{R_{d1}L_{d2}\left(C_d+C_g\right)} \\ &=\left(s+\omega_{Ld2,p1}\right)\cdot\left(s+\omega_{Ld2,p2}\right) \\ &=s^2+s2\xi\omega_n+\omega_n^2 \end{aligned} \tag{3.9}$$

where ξ and ω_n are the damping factor and the corner frequency of the complex poles, respectively. Note that the frequency response can be affected by the value of ξ. For ξ smaller than $1/\sqrt{2}$, a gain-peaking characteristic can be observed at around ω_n. Therefore, the bandwidth can be enhanced not only by zero but also complex poles. Under $R_{d1}= R_{d2}$ and $C_g= 3C_d$, the required inductance L_{d2} and the maximum achievable 3-dB bandwidth ω_{Ld2} can be derived from the equation $|z_{Ld2}(\omega_{Ld2})|^2= 1/2$ with $\omega_0= 1/(2R_{d1}C_d)$ [38]:

$$L_{d2}=m_{d2}\cdot R_{d1}^2\cdot C_d \tag{3.10}$$

where m_{d2} is 1.50, and the resulted ω_{Ld2} equals 1.46, as shown in Fig. 3.4, curve *f*. The improved bandwidth mainly results from the in-band ω_{z1} of 1.33, since the complex

poles have a $\xi_{Ld2,p1}$ of 0.79 which is larger than $1/\sqrt{2}$. Based on (3.8) ~ (3.10), ω_{z1}= $1/(1.5R_{d1}C_d)$= 1.33, $\omega_{Ld2,p1}$= $\omega_{Ld2,p2}$= $\sqrt{(1/(2L_{d2}C_d))}$= 1.15, and $\xi_{Ld2,p1}$= $(1/(4R_{d1}C_d)+R_{d2}/L_{d2})/(2\omega_n)$= 0.79. The properties of the poles and zeros as adding the three peaking inductors step by step are summarized in Table 3.1.

	without PIP	L_{d2}	L_{d2} + L_{s1}	L_{d2} + L_{s1} + L_{d1}
Zero	—	$\omega_{z1}=1.33$	$\omega_{z1}=1.33$	$\omega_{z1}=1.33$ $\omega_{z2}=2.50$
Pole	$\omega_{p1}=1.00$	—	—	$\omega_{Ld1,p3}=1.39$
Complex pole	—	$\omega_{Ld2,p1}=\omega_{Ld2,p2}$ $=1.15$	$\omega_{Ls1,p1}=\omega_{Ls1,p2}$ $=1.21$ $\omega_{Ls1,p3}=\omega_{Ls1,p4}$ $=2.37$	$\omega_{Ld1,p1}=\omega_{Ld1,p2}$ $=1.28$ $\omega_{Ld1,p4}=\omega_{Ld1,p5}$ $=3.01$
Damping factor	—	$\xi_{Ld2,p1}=0.79$	$\xi_{Ls1,p1}=0.82$ $\xi_{Ls1,p3}=0.28$	$\xi_{Ld1,p1}=0.63$ $\xi_{Ld1,p4}=0.14$

Table 3.1. Properties of the poles and zeros of one gain stage with PIP under different numbers of peaking inductors.

After obtaining the required L_{d2}, the inductance L_{s1} can be derived from (3.6) by setting L_{d1}= 0. The normalized transfer function $z_{Ls1}(s)$ includes additional complex poles of $\omega_{Ls1,p3}$ and $\omega_{Ls1,p4}$. To derive the required inductance and the maximum enhanced bandwidth ω_{Ls1}, (3.10) is used. A similar equation for L_{s1} can be obtained as:

$$L_{s1} = m_{s1} \cdot R_{d1}^2 \cdot C_d \tag{3.11}$$

where m_{s1} is 0.86, and the associated ω_{Ls1} equals 2.55 with a gain variation of 0.5 dB, as shown in Fig. 3.4, curve *g*. The bandwidth is improved mainly by both the in-band ω_{z1} of 1.33, and the additional complex poles with a $\xi_{Ls1,p3}$ of 0.28 and a $\omega_{Ls1,p3}$ ($\omega_{Ls1,p4}$) of 2.37. The above values are determined based on the denominator of $z_{Ls1}(s)$.

To derive the inductance L_{d1} for a maximum achievable bandwidth ω_{Ld1}, the

previously obtained L_{d2} and L_{s1} are both taken into account. With the normalized (3.6) by the DC impedance $R_{d1}//R_{d2}$ and (3.10) ~ (3.11), the derived result is:

$$L_{d1} = m_{d1} \cdot R_{d1}^2 \cdot C_d \tag{3.12}$$

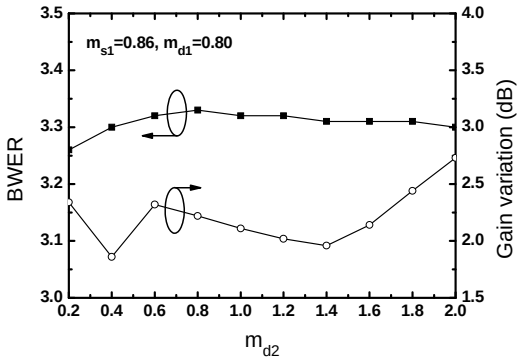
where m_{d1} is 0.80, and the resulted ω_{Ld1} equals 3.31 with a gain variation of 2.0 dB, as shown in Fig. 3.4 curve *h*. The first gain peaking at around ω_0 is due to the complex poles with a $\xi_{Ld1,p1}$ of 0.63 and the in-band zero ω_{z1} of 1.33, while the second peaking at around $3\omega_0$ results from the complex poles with a $\xi_{Ld1,p4}$ of 0.14 and the in-band zero ω_{z2} of 2.50. The zero ω_{z2} of 2.50 is calculated from R_{d1}/L_{d1}.

3.4.3 Design Trade-Offs in PIP Configuration

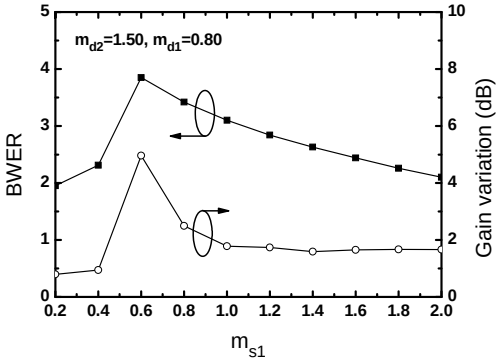
The above analysis illustrates the impact of each PIP inductor on the BWER and gain variation under the condition $R_{d1}= R_{d2}$ and $C_g= 3C_d$. It is also of interest to investigate the circuit performance if using different values of m_{d2}, m_{s1}, m_{d1}, C_g/C_d, and R_{d1}/R_{d2}, which provides guidelines toward the optimal design and a deeper understanding of the PIP configuration.

Fig. 3.5 shows the impact of each PIP inductor on the frequency response under $R_{d1}= R_{d2}$ and $C_g= 3C_d$. Under a fixed m_{s1} of 0.86 and m_{d1} of 0.80, the BWER is not a strong function of m_{d2} in the range of 0.2 ~ 2.0, as shown in Fig. 3.5(a). The highest BWER of 3.33 can be obtained at $m_{d2}= 0.8$ with a gain variation of 2.2 dB. In Fig. 3.5(b), with an m_{s1} of 0.6, the BWER and the gain variation both reach the highest values of 3.85 and 5.0 dB, respectively. Although the bandwidth can be greatly improved, the signal distortion may be serious because of the large gain variation. In the range of 0.8 ~ 1.2, the gain variation is kept below 2.5 dB with a BWER larger than 2.84, which is more suitable for a practical design. The dependence of the BWER and gain variation on m_{d1} is illustrated in Fig. 3.5(c). For a lower gain variation while

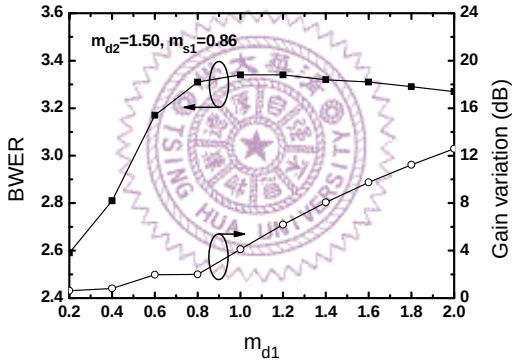
maintaining a high BWER, a better choice of m_{d1} should be around 0.8. Considering the trade-offs between a large BWER and a small gain variation, the previously obtained values of m_{d2}= 1.50, m_{s1}= 0.86, and m_{d1}= 0.80 are very close to the optimal result.



(a)



(b)

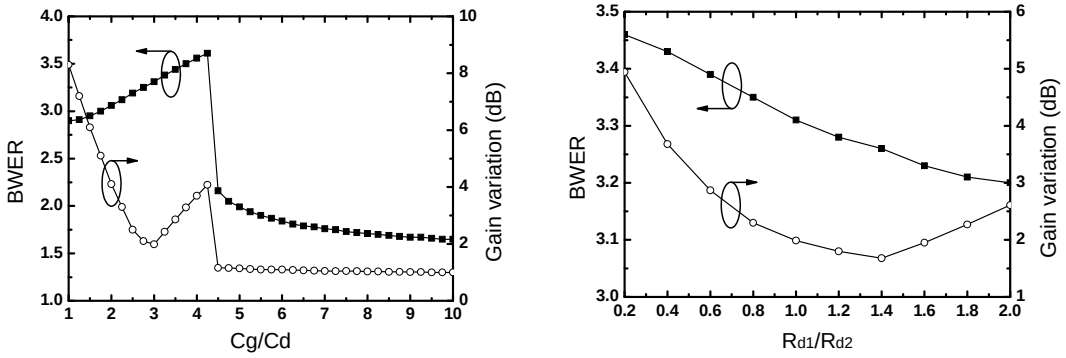


(c)

Fig. 3.5. The BWER and gain variation with different PIP inductors (a) m_{d2}, (b) m_{s1}, and (c) m_{d1}.

Fig. 3.6 plots the BWER and gain variation as a function of C_g/C_d and R_{d1}/R_{d2}. In more general cases, C_g/C_d could vary from 1 to 10 for different circuit topologies or extra source/load capacitances [31]. Within the range of 2.5 to 3.5 of C_g/C_d, high BWER values in a range of 3.15 ~ 3.46 can be achieved in a gain variation between 2.0 dB and 3.0 dB, as shown in Fig. 3.6(a). On the other hand, the BWER reduced monotonically as R_{d1}/R_{d2} increases as shown in Fig. 3.6(b). For a small R_{d1}/R_{d2} of 0.2, the BWER can be

as high as 3.46 but with a gain variation up to 4.94 dB. The gain variation can be reduced to 1.68 dB with a smaller BWER of 3.26 by choosing a R_{d1}/R_{d2} of 1.4. The selected R_{d1}/R_{d2} of 1 in the final design is simple and around the optimal value for both BWER and gain flatness.



(a) (b)

Fig. 3.6. The BWER and gain variation for different values of (a) C_g/C_d and (b) R_{d1}/R_{d2}.

TSING HUA UNIVERSITY

3.5 Summary

An effective wideband technique, PIP, was proposed, and the design concept and methodology were also presented in detail. With three inductors, a large BWER of 3.31 can be obtained based on considering the parasitic capacitance ratio in a practical transistor. This promising technique will be employed to design a 40-Gb/s TIA using 0.18-μm CMOS technology, and the details are shown in Chapter V.

Chapter IV: Design of a 24-GHz Balanced Amplifier

The proposed PPR technique with three external inductors is employed here to design a 24-GHz balanced amplifier. The design details and results will be shown as follows.

4.1 Circuit Topology

To achieve a high-gain performance, eight cascaded CS stages are adopted, as shown in Fig. 4.1. The PPR technique is incorporated into each stage to boost the amplifier gain up to A_0^8. In this cascade configuration, L_{ds} and L_{gs} from the next stage (see Fig. 2.2) can be combined to be one inductor L_{DD}, as shown in the figure. To simplify the circuit design and layout complexities, each CS stage is designed to be identical. Note that the required PPR inductor L_{gs} at the gate terminal of M_1 is removed, while one additional L_{gs} is inserted at the drain terminal of M_8. In this manner, the overall gain is comparable, and the layout of each CS stage is exactly the same. By connecting L_{DD} to the power supply voltage V_{DD}, each transistor is biased at V_{GS}= V_{DS}= V_{DD}. For the operation frequency f_o designed at 24 GHz, the component values are listed as follows: L_{DD}= 1.08 nH, L_{GD}= 0.54 nH, C_M= 52 fF, and the gate width W_g= 64 μm.

The capacitor C_M is implemented by a metal-insulator-metal (MIM) capacitor with a chip area of 6 μm × 6 μm. By using the EM simulator [39], L_{GD} was designed with a top metal width (W) of 1.5 μm, metal spacing (S) of 1.5 μm, number of turns (N) of 4.75, and inner radius (IR) of 5 μm, as shown in Fig. 4.2(a). The inductor shown in Fig. 4.2(b) features a W= 1.5 μm, S= 1.5 μm, N= 4.5, and IR= 5 μm, and two identical inductor are connected in series to form L_{DD}. By designing L_{DD} in this manner, the interconnects

between two stages can be shortened. The signal loss of the line can be reduced, and then the gain of the amplifier can be increased.

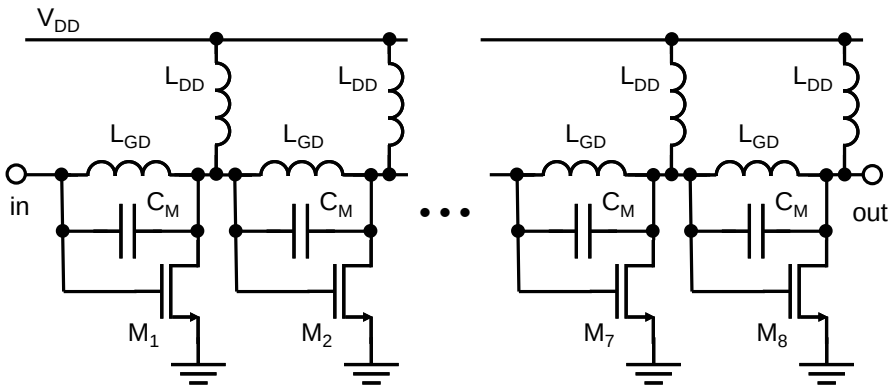
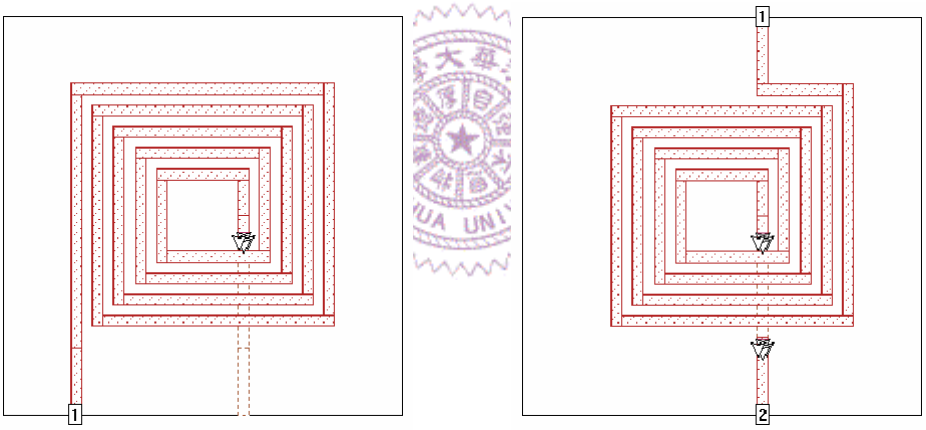


Fig. 4.1. Circuit topology of the single amplifier of each branch in the balanced amplifier (BA) configuration.



(a) (b)

Fig. 4.2. Top-view of the on-chip spiral inductors for (a) L_{GD} and (b) $L_{DD}/2$.

At the resonant frequency, the input and output impedances of the amplifier can be very large due to the PPR design. Therefore, the matching network designed by *LC* or transmission line becomes difficult for such a high transformation ratio. In this design, the BA configuration is adopted [40]-[41], which can not only match the input and output impedances to 50 Ω but also improve the circuit stability.

A standard BA is composed of two 90-degree couplers and two identical amplifiers

(Amp1 and Amp2), as illustrated in Fig. 4.3, where the input signal is divided into two parts by the input coupler with an equal power splitting but a 90-degree phase difference. Both signals are amplified separately in each path and then combined by the output coupler with a reversed 90-degree phase shift to obtain the overall output. In principle, the gain of a BA is the same as a single amplifier. However, the stability and input/output impedance matching can be improved by the balanced design even if the single amplifier of each branch is highly mismatched and with a very high gain. Therefore, the single amplifier of each branch can be intentionally mismatched to achieve a better circuit performance. In addition, the 90-degree couplers ensure excellent isolation from the previous and/or the following stages for easy system integration. As shown in Fig. 4.3, the input power from port *in* is divided to be half with a 90-degree phase difference and delivered to ports *out1* and *out2*. Part of the signal can be reflected back due to impedance mismatch. After passing through the 90-degree coupler again, the reflected signals from both paths appearing at port *in* have a 180-degree phase difference, which can cancel each other resulting in an unconditionally matched condition at the input. On the other hand, the reflected signals with a 0-degree phase difference are superimposed at port *isolated* and terminated by a 50-Ω resistor R_M. Similarly, the output port also has a minimum reflection to guarantee the matching and stability. Compared with a single amplifier, the BA configuration needs two couplers and two amplifiers, resulting in larger power consumption and chip area. However, the output 1-dB gain compression point $P_{1dB,out}$ is 3-dB higher than that obtained from a single amplifier. In addition, even with one of the amplifiers fails, the circuit can still operate with a reduced gain by 6 dB. Note that the resistor R_M was realized by silicided P+ poly with a length of 13 μm and a width of 2 μm. The capacitor C_C was realized by four MIM capacitors connected in parallel, and each of them with a chip area of 10 μm × 10 μm.

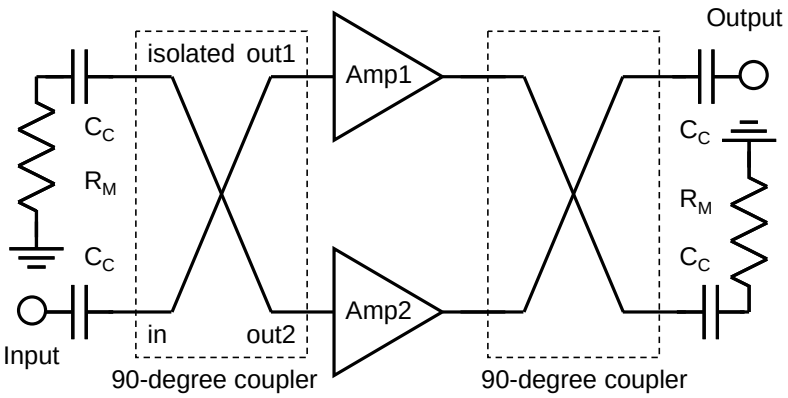
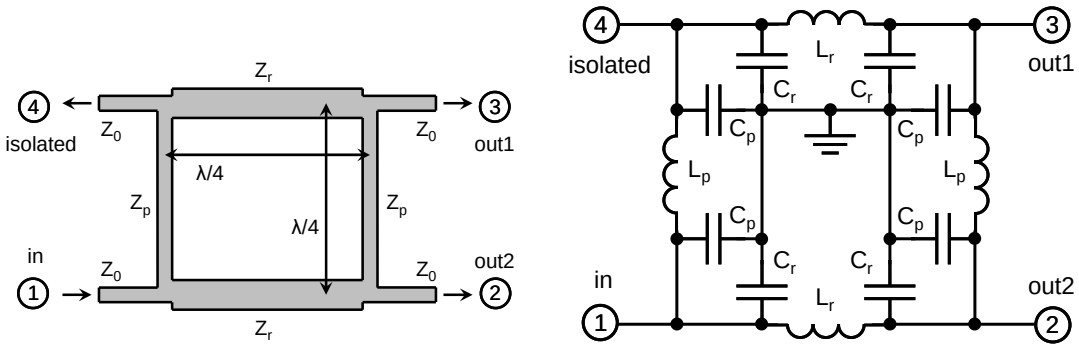


Fig. 4.3. Circuit topology of a BA.

4.2 Lumped-Element Coupler

The 90-degree couplers used for BA applications are usually realized by transmission lines, such as the branch-line coupler, as depicted in Fig. 4.4(a). The quarter-wavelength λ/4 transmission lines provide a 90-degree phase delay from port 1 to port 2, and a 180-degree delay from port 1 to port 3. The characteristic impedances of the series Z_r and the shunt Z_p transmission lines can determine the delivered power ratio of the two output ports. For an equal power splitting, Z_r and Z_p should be designed as $Z_0/\sqrt{2}$ and Z_0, respectively, where Z_0 is the characteristic impedance of the system, and is typically 50 Ω. For a design at 24 GHz, the calculated physical length of a quarter-wave microstrip line is about 1560 μm in the CMOS technology used here, which makes the balanced design with two couplers consuming a large chip area.



(a) (b)

Fig. 4.4. The 90-degree couplers in (a) branch-line and (b) lumped-element topologies.

In this work, the lumped-element coupler constructed from spiral inductors and MIM capacitors as shown in Fig. 4.4(b) is adopted [42]-[43]. Compared to the transmission-line coupler, this design is more area-efficient but has a smaller bandwidth. With the same function of the branch-line coupler, each λ/4 transmission line section can be replaced by a *LC* π-network including one inductor *L* and two capacitors *C* in the miniaturized lumped-element coupler. Using ABCD-parameters, the required *L* and *C* can be determined by the following equations for both series and shunt lines, where the matrix at the left-side is for a lossless λ/4 transmission line, and the matrix at the right-side is for the equivalent *LC* π-network. For the series line:

$$\begin{bmatrix} \cos\theta & jZ_r \sin\theta \\ j\dfrac{1}{Z_r}\sin\theta & \cos\theta \end{bmatrix} = \begin{bmatrix} 1-\omega_o^2 L_r C_r & j\omega_o L_r \\ j\omega_o C_r\left(2-\omega_o^2 L_r C_r\right) & 1-\omega_o^2 L_r C_r \end{bmatrix} \tag{4.1}$$

where θ is 90-degree, and for the shunt branch line, a similar equation can be constructed as shown below:

$$\begin{bmatrix} \cos\theta & jZ_p \sin\theta \\ j\dfrac{1}{Z_p}\sin\theta & \cos\theta \end{bmatrix} = \begin{bmatrix} 1-\omega_o^2 L_p C_p & j\omega_o L_p \\ j\omega_o C_p\left(2-\omega_o^2 L_p C_p\right) & 1-\omega_o^2 L_p C_p \end{bmatrix} \tag{4.2}$$

By solving the above two equations, the values of the lumped elements can be obtained as follows:

$$L_r = Z_r / \omega_o \tag{4.3}$$

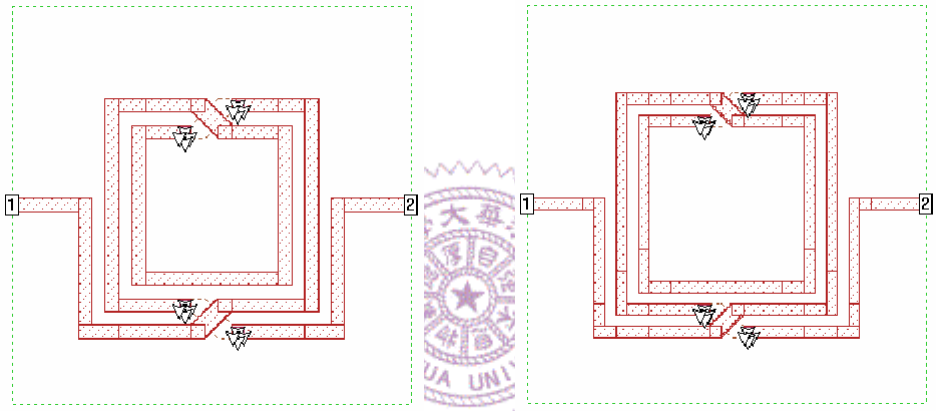
$$L_p = Z_p / \omega_o \tag{4.4}$$

$$C_r + C_p = \frac{1}{\omega_o}\left(\frac{1}{Z_r} + \frac{1}{Z_p}\right) \tag{4.5}$$

Note that C_r and C_p can be combined as one capacitor in circuit implementation since

these two capacitors are connected in parallel.

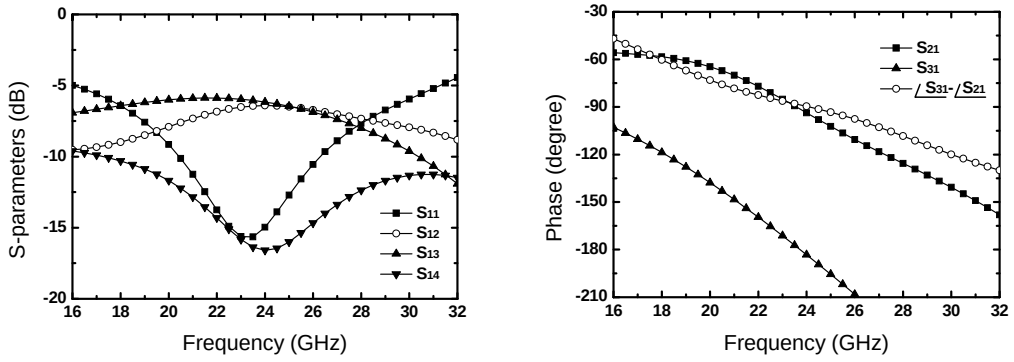
By considering the parasitic effects of both the L and C, the finally optimized component values of the 24-GHz lump-element coupler are listed as follows: L_r= 0.23 nH, L_p= 0.33 nH, and C_r+ C_p= 110 fF, where C_r and C_p are implemented by a MIM capacitor with a chip area of 9.5 μm × 9.5 μm. The inductor L_r features a W= 2 μm, S= 2 μm, N= 1.5, and IR= 10 μm, as shown in Fig. 4.5(a), and L_p features a W= 2 μm, S= 2 μm, N= 1.5, and IR= 14 μm, as shown in Fig. 4.5(b). The total chip area is ~ 200 μm × 200 μm, which occupies an area of only ~ 2 % compared to that of the conventional branch-line coupler using the same technology.



(a) (b)

Fig. 4.5. Top-view of the on-chip spiral inductors for (a) L_r and (b) L_p.

The simulated S-parameters based on the actual layout of the lumped-element coupler are shown in Fig. 4.6. At 24 GHz, the insertion losses from port 1 to port 2 and port 3 are 6.4 dB and 6.2 dB, respectively. The loss is higher than the desired value of 3 dB due to the resistive loss introduced from the spiral inductors. The reflection coefficients of port *in* and the isolation from port *in* to port *isolated* are both below -15 dB. The phase difference between the two output ports is 89.6 degree.



(a) (b)

Fig. 4.6. Simulated S-parameters of the 24-GHz lumped-element coupler for (a) magnitude and (b) phase.

4.3 Design of Interconnects

Special care had been taken for the layout of the circuit. For high-frequency circuits, the commonly used interconnect structures are microstrip (MS) line and coplanar waveguide (CPW), as shown in Fig. 4.7(a) and (b) respectively. However, these two structures can suffer either from severe signal crosstalk or significant signal loss from the lossy silicon substrate [44]. As shown in Fig. 4.7(c), the grounded-CPW (GCPW) configuration can be employed to prevent the above problems [45]-[46]. The sidewall and bottom ground planes realized by various metal layers are utilized for a better shielding of the signal paths.

To further improve the signal loss, a new transmission line structure, semi-coaxial (SC) line, is proposed, which demonstrates a superior low-loss performance [47]. By using a semi-rounded ground plane, as shown in Fig. 4.7(d), the SC lines also provide a perfect shielding of the signal lines from the crosstalk and the lossy substrate to achieve a low-loss characteristic over a wide frequency range. A lower signal loss characteristic is expected since the semi-coaxial structure can support a wave propagation more close to the TEM mode. The measured attenuation constant of the SC line presented the lowest value of 0.90 dB/mm at 50 GHz compared to 5.04 dB/mm of MS line [48], 1.22

dB/mm of CPW [48], and ~ 1.00 dB/mm of GCPW [45].

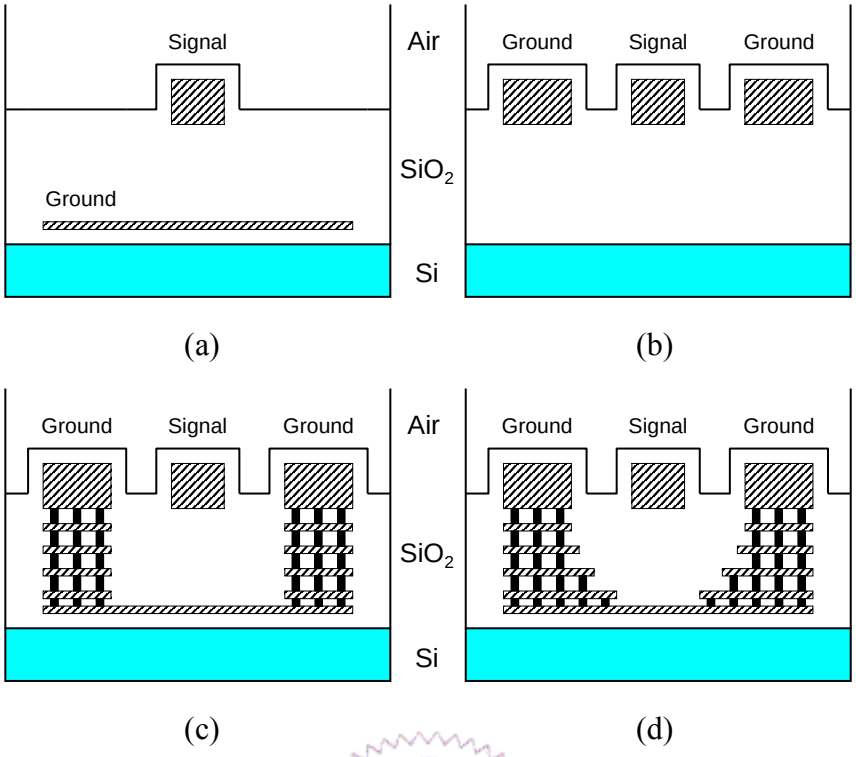


Fig. 4.7. RF interconnect structures for (a) MS line, (b) CPW, (c) GCPW, and (d) SC line in a standard 1P6M CMOS process.

TSING HUA UNIVERSITY

4.4 Stability Issues

For such a high gain amplifier, stability is a critical design consideration. To achieve unconditional stability, the stability factor K and the stability measure B_1 should be larger than 1 and 0, respectively [49]. The simulation results indicate that each inter-stage and the whole circuit are unconditionally stable over a wide frequency range. The amplifier also shows unconditional stability under the V_{DD} varying in a range of 0.6 V to 1.8 V, as shown in Fig. 4.8. Note that the inter-stage stability is verified by the S-probe in the simulation tool ADS [50]. For an unconditional inter-stage stability, StabIndex1 and StabIndex2 should both be smaller than 1, as shown in Fig. 4.9. The simulation results indicate that each inter-stage is unconditionally stable over a wide frequency range, as shown in Fig. 4.10. Note that eight CS stages were employed for a high-gain amplification.

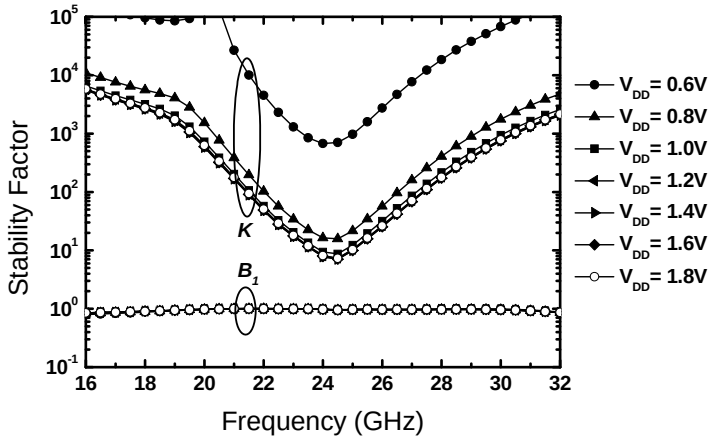


Fig. 4.8. Simulated stability factor and stability measure of the whole BA with different supply voltages.

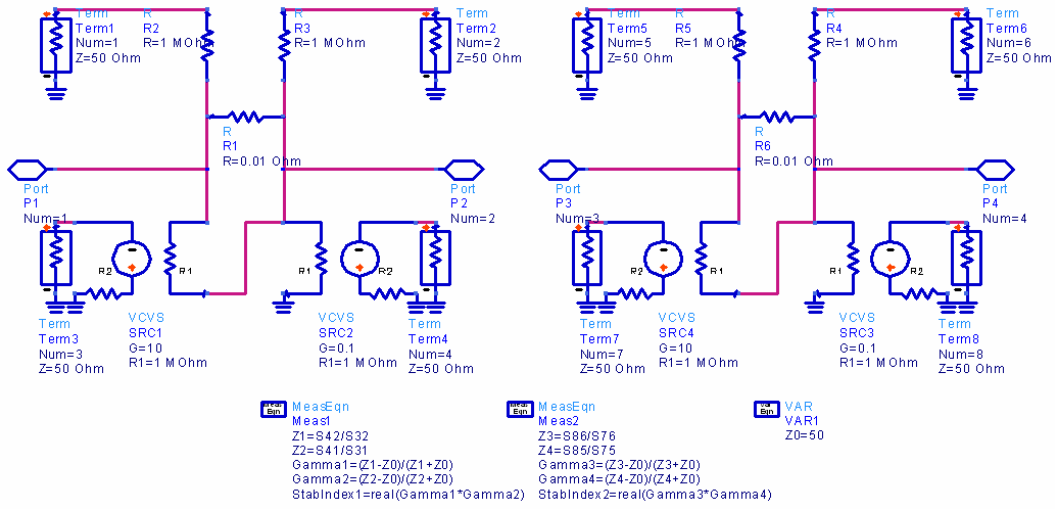


Fig. 4.9. Circuit schematic of S-probe for measuring the inter-stage stability.

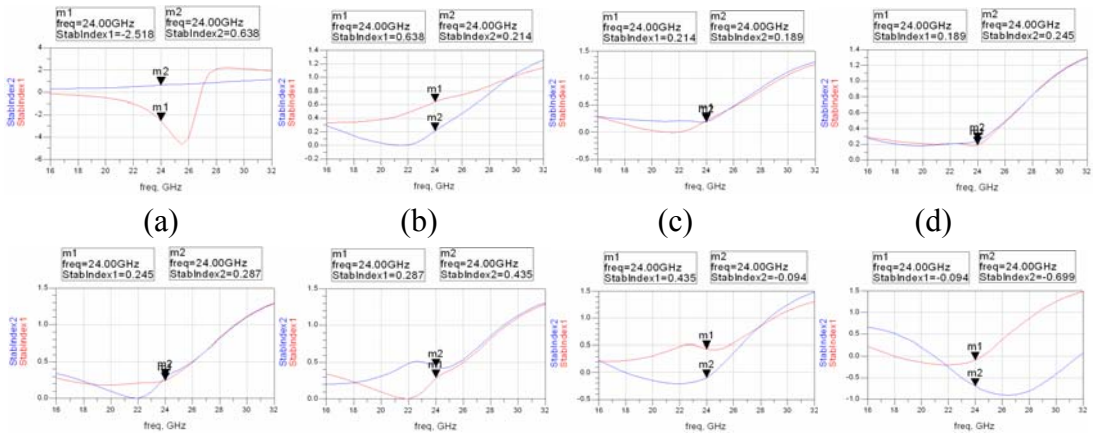


Fig. 4.10. Frequency responses of the inter-stage stability for (a) 1st, (b) 2nd, (c), 3rd, (d) 4th, (e) 5th, (f) 6th, (g) 7th, and (h) 8th stage of the amplifier shown in Fig. 4.1.

4.5 Measured Frequency Responses

The fully-integrated BA was fabricated in the 0.18-μm CMOS technology with a chip area of 0.97 × 0.63 mm^2 including the probing pads (core area: 0.78 × 0.43 mm^2), as shown in Fig. 4.11. The chip was measured on-wafer by using coplanar ground-signal-ground (GSG) probes (Picoprobe 67A-GSG-125-C-W). Fig. 4.12 shows the measured S-parameters, where the gain S_{21} at 24 GHz is 41.6 dB, and the peak gain G_p is 45.0 dB at the frequency f_p of 23.7 GHz. The S_{11} and S_{22} at f_p are -10.8 dB and -9.1 dB, respectively, which indicate a good input/output matching. From the measured S-parameters, the amplifier is unconditionally stable over the measured frequency range from 16 GHz to 32 GHz, as shown in Fig. 4.13.

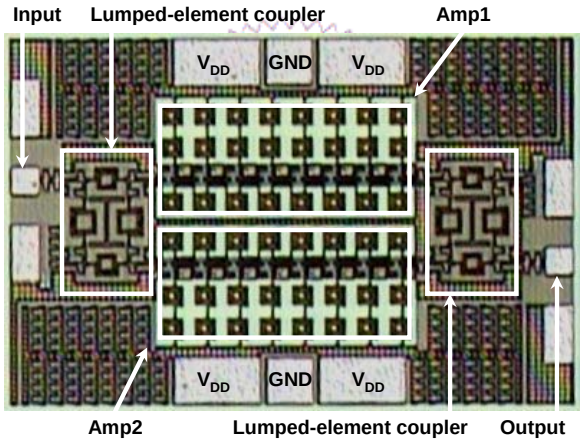


Fig. 4.11. Chip micrograph for the 24-GHz BA, and the chip size including the probing pads is 0.97 × 0.63 mm^2 (core area: 0.78 × 0.43 mm^2).

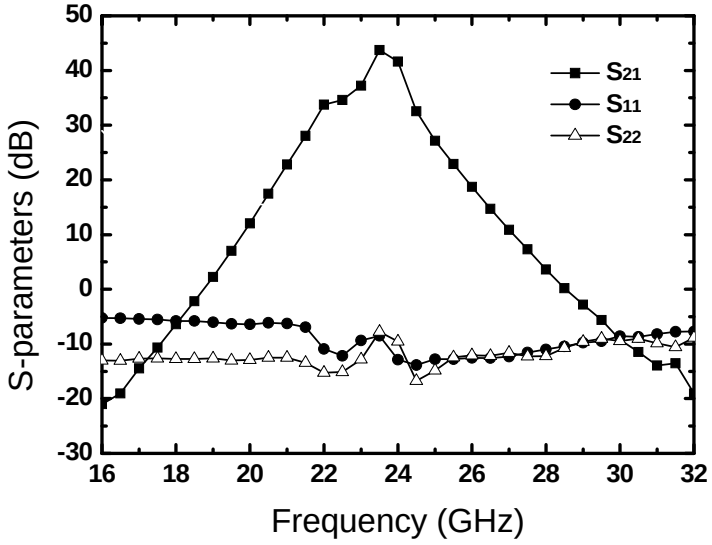


Fig. 4.12. Measured S-parameters as a function of frequency.

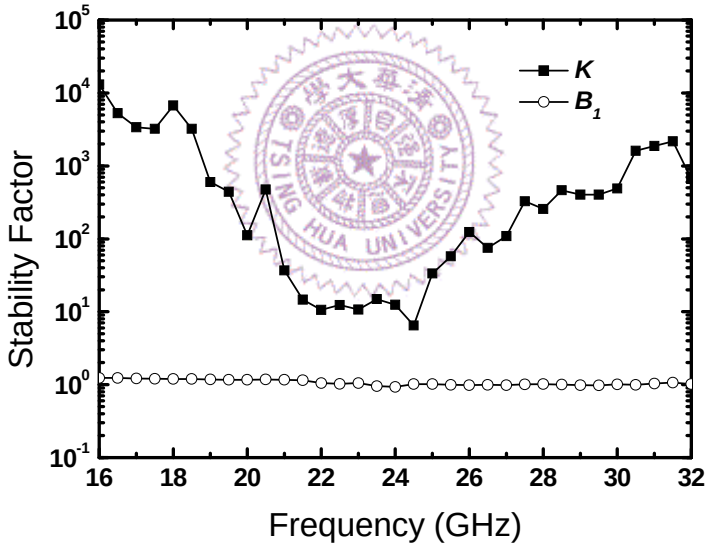


Fig. 4.13. Measured stability factors as a function of frequency.

The noise figure (*NF*) of BA was measured and simulated from 16 GHz to 26.5 GHz as shown in Fig. 4.14. A good agreement between measured and simulated *NF* is obtained. As can be seen, the amplifier shows relatively large *NF* of 9.4 dB and 10.8 dB respectively for the simulated and measured values at f_p. The *NF* of the coupler and the single amplifier are also presented for further analysis, which are 3.3 dB and 5.8 dB (at

f_p), respectively. The 3.3 dB can be attributed to the insertion loss of the lumped-element coupler (~ 6.3 dB), which is 3.3 dB higher than that of an ideal coupler. A possible solution for reducing *NF* of the proposed BA is to optimize the lossy lumped-element coupler. If an ideal insertion loss of 3 dB can be achieved, the measured *NF* can be reduced to ~ 7.5 dB. The output power level as a function of the input power was measured at f_p, which indicated a $P_{1dB,\ out}$ of -2.3 dBm, as shown in Fig. 4.15. Under a supply voltage of 1 V, the power consumption (P_{DC}) is 123 mW. By employing the proposed PPR technique, a high peak gain-frequency product per DC power ($G_p f_p/P_{DC}$) figure-of-merit of 34.3 GHz/mW and a high $G_p f_p/(NF \times P_{DC})$ of 2.9 GHz/mW can be achieved.

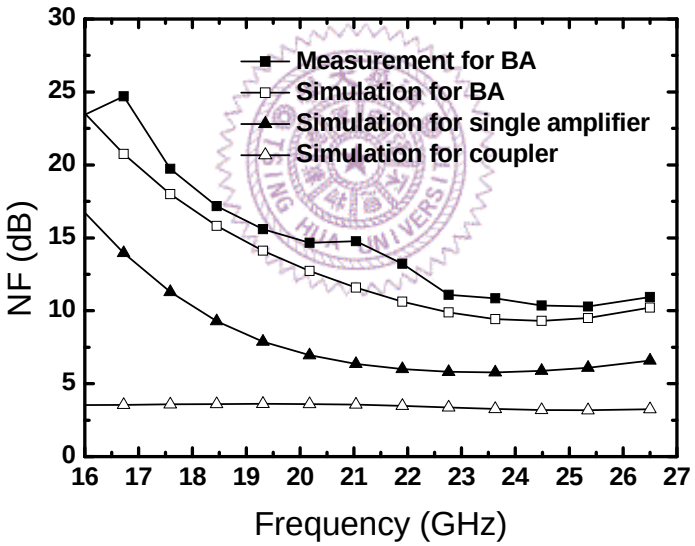


Fig. 4.14. Measured and simulated *NF* as a function of frequency.

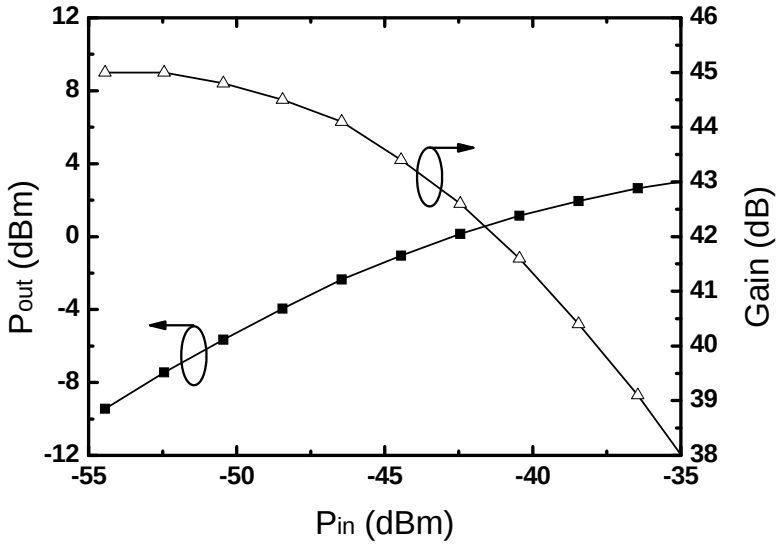


Fig. 4.15. Measured output power and gain versus input power at the peak gain frequency (f_p).

The circuit performances of the proposed BA are summarized in Table 4.1 together with other works at similar operation frequencies [51]-[53]. Although the balanced-type design requires two amplifiers and couplers, the core area in this design is still very small (~ 0.34 mm^2) owning to the miniaturized lumped-element coupler. The proposed BA presented the highest gain and $G_p f_p / P_{DC}$ among the published results with similar technologies and operation frequencies.

Ref.	This work	[51]	[52]	[53]
G_p (dB)	45.0	15.0	10.0	8.9
f_p (GHz)	23.7	21.8	24.0	25.7
S_{11} (dB)	-10.8	-21.0	-14.0	-14.0
S_{22} (dB)	-9.1	—	—	-12.0
NF (dB)	10.8	6.0	6.0*	6.9
$P_{1dB,out}$ (dBm)	-2.3	-9.0	—	-2.3
V_{DD} (V)	1	1.5	—	1.8
P_{DC} (mW)	123	24	47	54
Chip area (mm^2)	0.97×0.63	—	—	1.05×0.7
Core area (mm^2)	0.78×0.43	0.2×0.25	—	—
$G_p f_p/P_{DC}$ (GHz/mW)	34.3	5.1	1.6	1.3
$G_p f_p/(NF \times P_{DC})$ (GHz/mW)	2.9	1.3	0.4	0.3
Process	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS

* Extrapolated from measured results up to 20 GHz.

Table 4.1. BA Performance summary and comparison with other works.

4.6 Summary

A fully-integrated CMOS BA was presented, and demonstrated a gain of 45.0 dB at around 24 GHz with an unconditional stability. The input and output ports were both matched well. Under a supply voltage of 1 V, *NF* and $P_{1dB,\,out}$ were 10.8 dB and -2.3 dBm, respectively. With the proposed PPR design technique and the employment of the lumped-element couplers, the proposed BA showed the highest $G_p f_p/P_{DC}$ figure-of-merit of 34.3 GHz/mW among the published results.

Chapter V: Design of a 40-Gb/s Transimpedance Amplifier

Being the first block of a receiver chain, TIA plays an important role to amplify the weak high-speed signal from the photo detector. With a target speed of 40-Gb/s, the proposed PIP technique is utilized to boost the performance of the transistor with a gate length of 0.18 μm. The design details and results are addressed as follows.

5.1 Circuit Topology

To demonstrate the proposed PIP technique, a TIA targeting at 40-Gb/s is realized in 0.18-μm CMOS technology. The 40-Gb/s TIA composes of four cascaded CS stages, as shown in Fig. 5.1. For a cascaded amplifier with identical 1st-order gain stages, the optimal stage number n_{opt} can be estimated by a simple equation of $2\times\ln(A_{tot})$ to achieve a maximized circuit bandwidth, where A_{tot} is the total voltage gain [54]. Note that A_{tot} is equivalent to the overall S_{21} under the matched input and output impedances of 50 Ω. For the proposed TIA with an A_{tot} of 16.7 dB, the finally designed stage number is 4. Identical resistance for the drain bias resistors R_D of each stage is employed, and the input and output impedances are designed as 50 Ω through the resistors $R_{M1} \sim R_{M4}$. Note that the 50-Ω input impedance is mainly for high-frequency measurement consideration, which may not be the optimal design if considering the electrical characteristics of the photodiode.

For a high-gain characteristic, a large R_D is preferred. However, the required peaking inductances for PIP topology, as derived in section 3.4.2, are proportional to R_D^2. It can be seen that a trade-off exists here since a large inductor not only occupies a large chip area but also causes difficulties to maintain an inductive characteristic up to

the circuit bandwidth. In addition, the resistive parasitics of the inductors can degrade the circuit performance. This effect is more obvious for the series-connected inductors L_{s1} in PIP configuration. In practical design, these inductors are designed to be smaller than the calculated values to reduce the resistive loss. The optimized R_D obtained for reasonable inductances while still providing high gain is 200 Ω. The adopted device width of $M_1 \sim M_3$ is 48 μm with a f_T of ~ 60 GHz and a f_{max} of ~ 90 GHz (estimated from the foundry provided transistor model), while a larger width of 64 μm is employed for M_4 to increase the gain and the output signal swing under a 50-Ω load. The inductances ($L_{P1} \sim L_{P9}$) are designed based on the derived equations (3.10) ~ (3.12), while some optimizations are essential due to the frequency dependence of C_g/C_d and the parasitic effects of the on-chip inductors. The finally designed values are L_{P1}= L_{P2}= 0.85 nH, L_{P3}= 0.48 nH, L_{P4}= L_{P5}= L_{P7}= L_{P8}= 1.6 nH, L_{P6}= 0.42 nH, and L_{P9}= 0.2 nH. Compared with the theoretical value, a smaller BWER of 2.88 (simulated) for the single-stage amplifier using PIP (one of the three identical stages in the final design, see Fig. 5.1) is obtained in actual implementation.

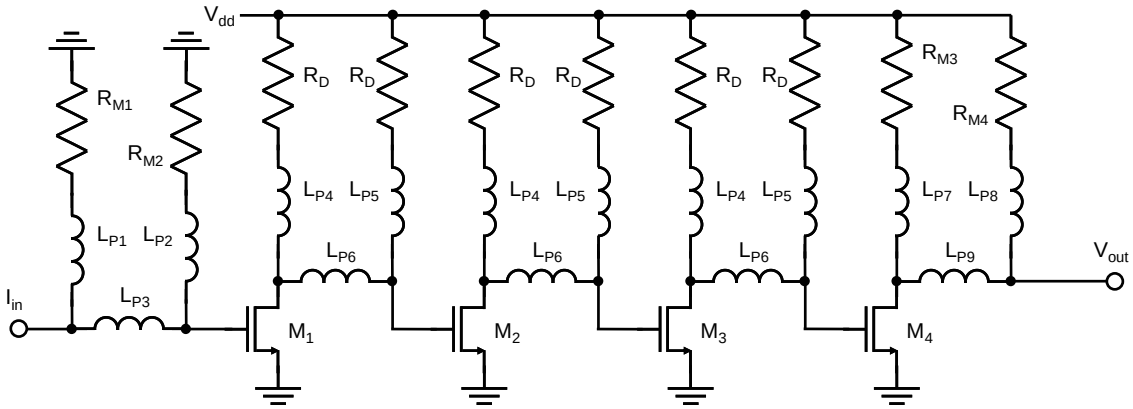


Fig. 5.1. Circuit topology of the proposed 40-Gb/s CMOS TIA with PIP.

The resistor R_D was realized by silicided P+ poly with a length of 47.2 μm and a width of 2 μm, and $R_{M1} \sim R_{M4}$ with a length of 47.2 μm and a width of 4 μm. The

inductor L_{P1} and L_{P2} were designed with a W= 2 μm, S= 4 μm, N= 4.5, and IR= 8 μm, as shown in Fig. 5.2(a). The inductor L_{P3} features a W= 5 μm, S= 5 μm, N= 2.5, and IR= 15 μm, as shown in Fig. 5.2(b). The inductor L_{P4}, L_{P5}, L_{P7}, and L_{P8} feature a W= 1.5 μm, S= 3 μm, N= 4.5, and IR= 15 μm, as shown in Fig. 5.2(c). The inductor L_{P6} features a W= 2 μm, S= 4 μm, N= 3.5, and IR= 8 μm, as shown in Fig. 5.2(d). The inductor L_{P9} features a W= 5 μm, S= 5 μm, N= 2.5, and IR= 10 μm, as shown in Fig. 5.2(e).

Fig. 5.3 compares the design of a TIA with and without using PIP technique. With a transimpedance gain Z_T of 51 dBΩ, the simulated bandwidth for the TIA with PIP is improved by a factor up to ~11 (33.8 GHz/ 3.1 GHz) compared to that without PIP. It is worth to point out that a photodiode capacitance C_{pd} of 50 fF is incorporated at the TIA input monolithically by the MIM capacitor in CMOS process, which is also the main limitation for the TIA bandwidth. A value of 50 fF was determined by the following manner. For a high-speed operation, it is essential to use a photodiode with a smaller C_{pd}. From the datasheet of two commercial photodiodes operating up to 50 GHz, the parasitic capacitance can be extracted from the output reflection coefficient S_{22} [55]. With an output impedance of 50 ohm, the capacitance of the photodiode is ~ 42 fF (u2t XPDV2020R, S_{22}= -10 dB) and 64 fF (u2tXPDV2040R, S_{22}= -7 dB). Therefore, a C_{pd} of 50 fF is a reasonable value to be used as the input loading of the TIA. By employing the PIP configuration (L_{P1} ~ L_{P3}) at the input stage, the capacitive loading from C_{pd} can be effectively resonated to achieve a wide bandwidth.

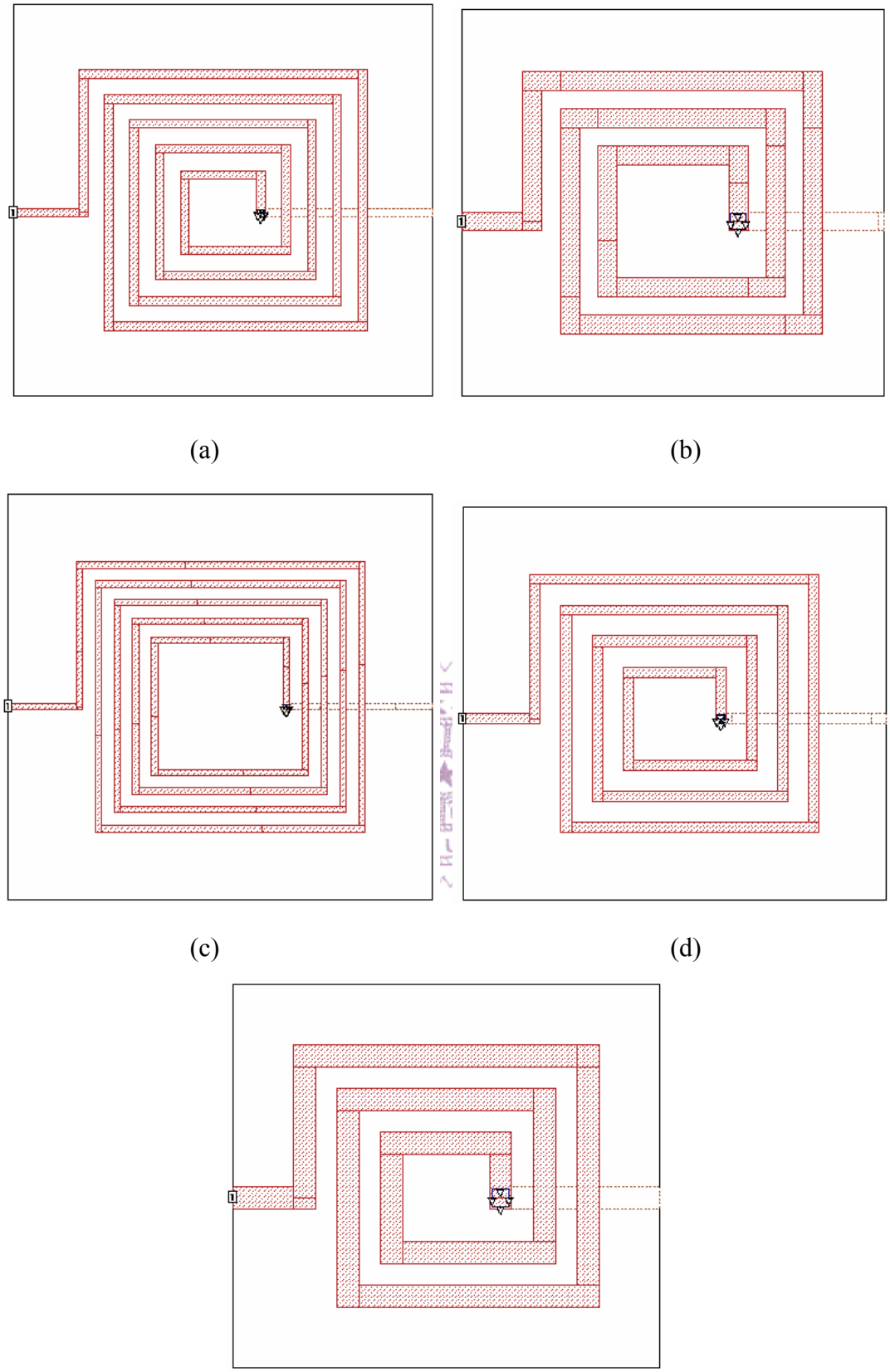


Fig. 5.2. Top views of the spiral inductors for (a) L_{P1} and L_{P2}, (b) L_{P3}, (c) L_{P4}, L_{P5}, L_{P7}, and L_{P8}, (d) L_{P6}, and (e) L_{P9}.

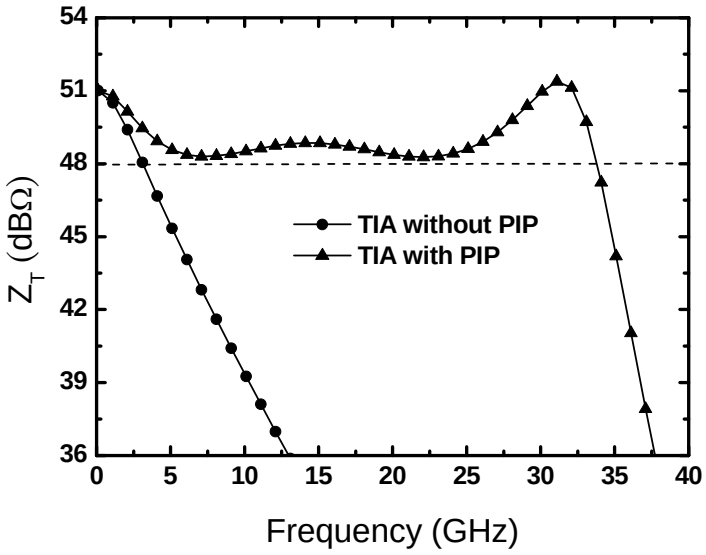


Fig. 5.3. Simulated frequency response for the TIA with and without PIP.

The impact of the corner-case transistors (slow and fast) on the frequency response of the TIA is simulated and shown in Fig. 5.4. For the slow case, the gain is reduced to 47.8 dBΩ and the bandwidth is increased to 34.1 GHz. On the other hand, the gain is increased to 52.2 dBΩ and the bandwidth is decreased to 33.7 GHz for the fast case.

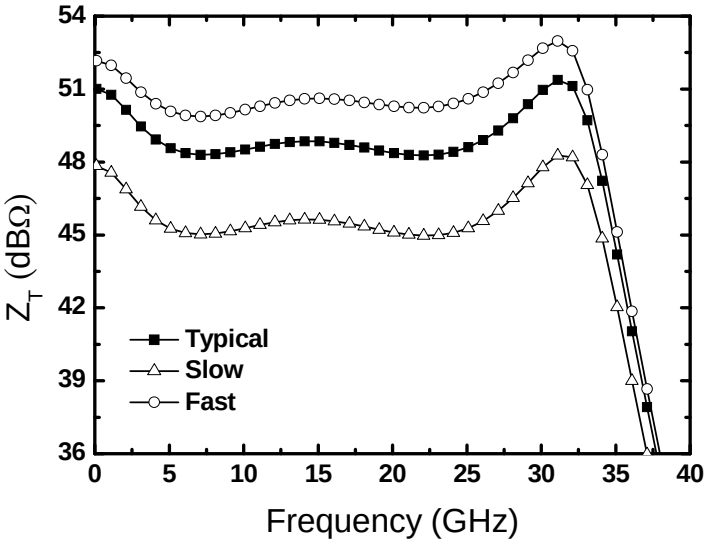


Fig. 5.4. Simulated impact of corner-case transistors on the frequency response of the proposed TIA.

In this design, GCPW configuration was employed for the interconnects. The total length of the signal paths in the designed TIA is about 500 μm, which has an insertion loss of only 1.1 dB at 33.8 GHz estimated using the EM simulator. In addition, the lines were all designed as 50-Ω to alleviate the additional capacitive loading effect on the circuit.

5.2 Noise Analysis

The input-referred noise current $i_{n,in}$ is an important issue for TIA design, which determines the sensitivity of the circuit. For the cascaded configuration, the input-referred noise is dominated by the first stage, since the impact of the noise from the later stages is reduced through the gain of the previous stages. In the following analysis, only the first transistor M_1 and the input PIP network ($L_{P1} \sim L_{P3}$ and $R_{M1} \sim R_{M2}$) are considered, as shown in Fig. 5.5.

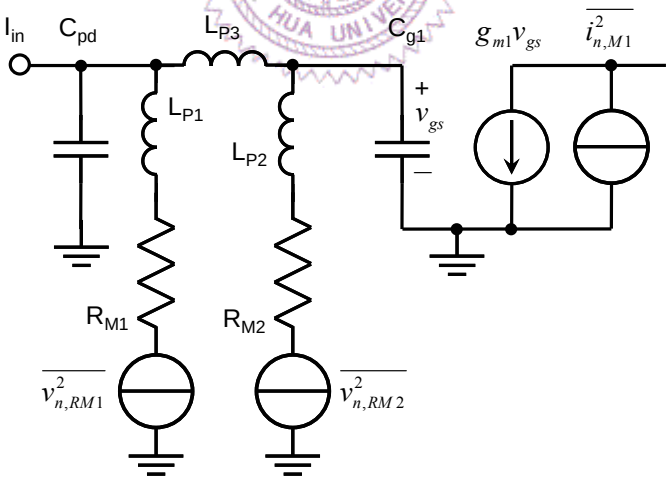


Fig. 5.5. Noise equivalent circuit model for the TIA input stage as shown in Fig. 5.1.

For 0.18-μm CMOS technology, previous studies indicate that the drain thermal noise dominates the device noise characteristics [56]-[57]. Based on this conclusion, the mean-square noise current spectral density can be derived as:

$$\overline{i_{n,in}^2} = 4kTR_{M1}\left|\frac{1}{Z_{RL1}}\right|^2 + 4kTR_{M2}\left|\frac{1}{Z_{RL2}} + sL_{P3}\left(\frac{1}{Z_{RL1}Z_{RL2}} + \frac{sC_{pd}}{Z_{RL2}}\right)\right|^2$$
$$+ \frac{4kT\gamma}{g_{m1}}\left|\frac{1}{Z_{RL1}} + \frac{1}{Z_{RL2}} + s\left(C_{pd} + C_{g1}\right) + sL_{P3}\left(\frac{1}{Z_{RL1}Z_{RL2}} + \frac{sC_{g1}}{Z_{RL1}} + \frac{sC_{pd}}{Z_{RL2}} + s^2C_{pd}C_{g1}\right)\right|^2 \quad (5.1)$$

where

$$Z_{RL1} = R_{M1} + sL_{P1}$$
$$Z_{RL2} = R_{M2} + sL_{P2} \quad (5.2)$$

where γ is the noise factor of the drain thermal noise, and g_{m1} and C_{g1} are the transconductance and the equivalent gate capacitance of M_1, respectively. As can be seen from the equation, the capacitance related terms increase the noise current as the frequency increases, while the rest of the terms result in an opposite trend owning to the inductive reactance in the denominator. The measured results as will be shown in section 5.3 indicate that the in-band noise current decreases with increased frequency. In other words, the capacitance related terms in (5.1) are not significant is the desired bandwidth. This trend can be attributed to the increased reactance of L with frequency, which provides relatively high impedances to block the noise currents generated from R_{M1}, R_{M2}, and M_1 to flow into the input terminal. Based on the above analysis, the PIP inductors at the input stage not only improve the bandwidth but also the noise performance in the desired band.

In addition to the noise current, the input-referred noise voltage is also derived. Since the input node is shorted to ground in this case, the noise contribution from R_{M1} and the impact from C_{pd} are both neglected. The derived equation can be written as:

$$\overline{v_{n,in}^2} = 4kTR_{M2}\left|\frac{sL_{P3}}{Z_{RL2}}\right|^2 + \frac{4kT\gamma}{g_{m1}}\left|1 + sL_{P3}\left(\frac{1}{Z_{RL2}} + sC_{g1}\right)\right|^2 \quad (5.3)$$

By combining the noise current and voltage, the derived NF can be written as:

$$NF = 1 + \frac{\left(\sqrt{\overline{i_{n,in}^2}} + \sqrt{\overline{v_{n,in}^2}}\, Y_s\right)^2}{4kT / R_s} \tag{5.4}$$

Since the above equation is too complex to simplify, the simulated result will be shown later.

5.3 Measured Frequency Responses

The TIA was fabricated in 0.18-μm CMOS technology with a chip area of 1.17 × 0.46 mm^2, as shown in Fig. 5.6. The TIA was measured on-wafer with coplanar ground-signal-ground (GSG) probes (Picoprobe 67A-GSG-125-C-W) for S-parameters, noise figure, and eye-diagram measurements.

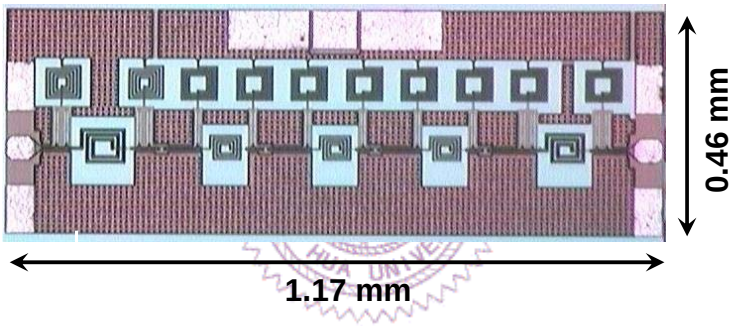


Fig. 5.6. Chip micrograph.

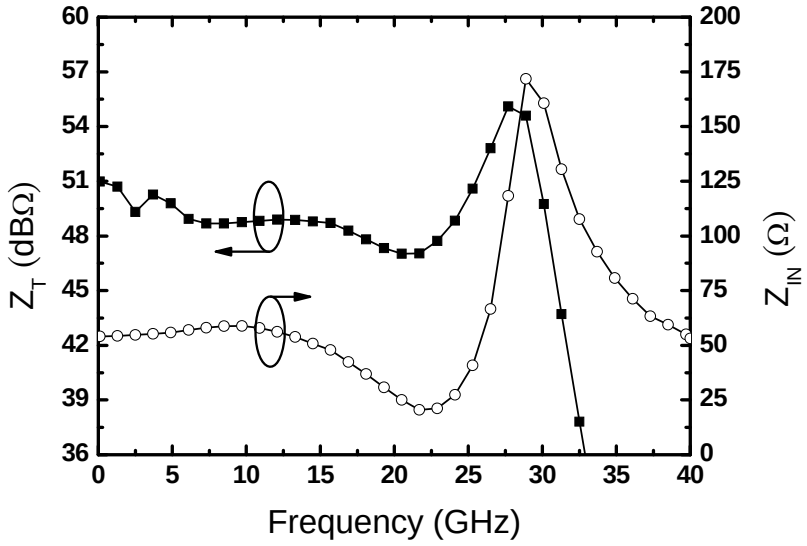


Fig. 5.7. Measured Z_T and Z_{IN}.

Using the network analyzer 8510C, the S-parameters were taken from 0.1 GHz to 40 GHz. The measured response of Z_T is shown in Fig. 5.7. The gain and the 3-dB bandwidth $f_{3\text{-}dB}$ are 51 dBΩ and 30.5 GHz in the presence of an on-chip C_{pd} of 50 fF at the input, respectively. The magnitude of the input impedance Z_{IN} is 54 Ω at low frequencies, but increases due to the PIP inductors at around $f_{3\text{-}dB}$. The measured S_{22} within the $f_{3\text{-}dB}$ is all below -10 dB, and S_{21} at low frequencies is up to 16.7 dB, as shown in Fig. 5.8.

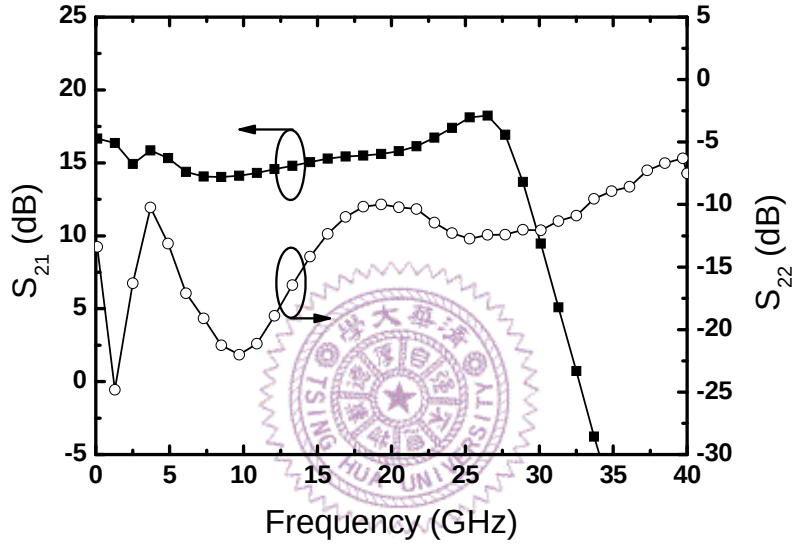


Fig. 5.8. Measured S_{21} and S_{22}.

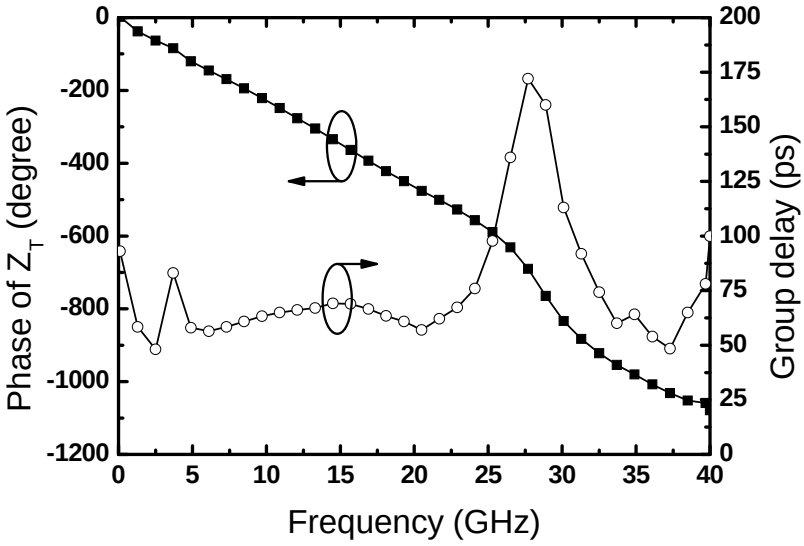


Fig. 5.9. Measured phase and group delay.

The phase of Z_T is linearly decreased with frequency and the group delay variation is below 45 ps up to 24 GHz, as illustrated in Fig. 5.9. Note that a trade-off exists between the bandwidth enhancement and the phase linearity. In this study, we mainly focus on bandwidth enhancement and thus the group delay variation increases. As will be observed from the eye diagrams of the TIA especially the one at 40-Gb/s (Fig. 5.12(d)), the signal smears and the rising and falling edges broaden due to the group delay variation with frequency, i.e. the phase velocity variation at different frequencies.

Using the noise figure analyzer N8975A, the noise figure (*NF*) was measured from 3.5 GHz to 26.5 GHz, as shown in Fig. 5.10. The value decreases from 11.9 dB to 6.7 dB as the frequency increases, which is in an excellent agreement with the simulated results.

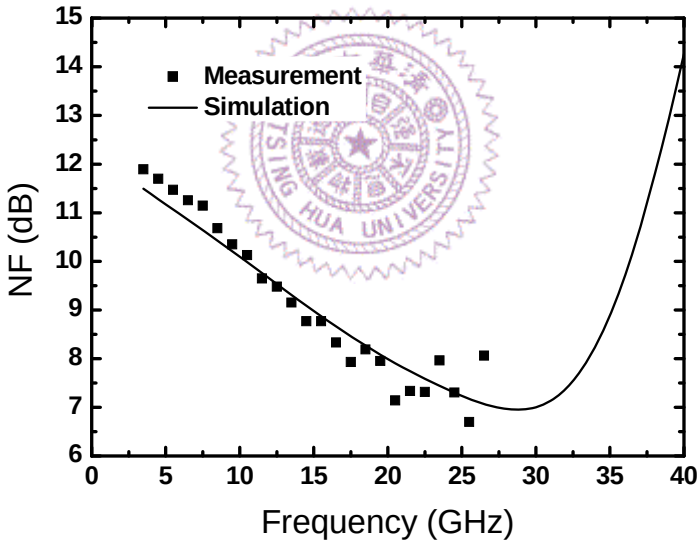


Fig. 5.10. Measured and simulated *NF*.

The noise characteristic of the TIA can be represented by a single noise current source referred to the input [58]:

$$\overline{i_{n,in}^2} = \frac{\overline{v_{n,outamp}^2}}{Z_T^2} \tag{5.5}$$

where $v_{n,outamp}$ is the output noise voltage of the amplifier. Based on the definition of *NF*,

the noise current can be extracted as shown in Fig. 5.11. Note that the calculation is under a 50-Ω condition, which is consistent with the measurement environment. Also, the calculation includes the effect of the input capacitor C_{pd} connected in front of the TIA. As can be seen, a decreasing noise current with frequency can be observed and a lowest value of 34.3 pA/√Hz at 25 GHz is obtained. Although not measured directly, the simulated results indicate that the capacitance related higher order terms in (5.1) become significant only at above ~ 30 GHz. To investigate the effect of C_{pd} on the noise characteristic, the simulated $i_{n,in}$ with different C_{pd} values is presented in Fig. 5.11. As predicted by (5.1), the capacitance related terms increase the noise current as the frequency increases. When a large C_{pd} is applied, the C_{pd}–related terms become dominant and the noise current increases with frequency.

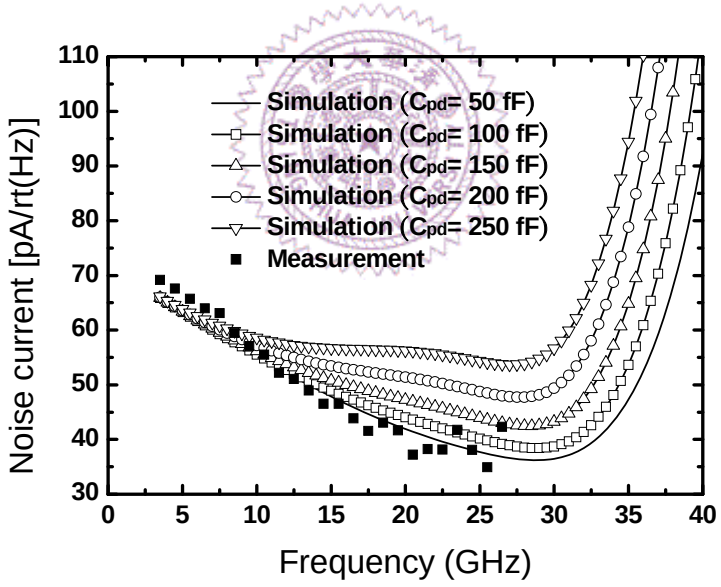


Fig. 5.11. Measured $i_{n,in}$ and the simulated $i_{n,in}$ with different values of C_{pd}.

In addition, the root-mean-square (RMS) noise current can be calculated as [59]:

$$i_{n,in}^{rms} = \frac{1}{R_T}\sqrt{\int_0^{>2f_{3-dB}} \left|Z_T(f)\right|^2 \cdot \overline{i_{n,in}^2}(f)df} \tag{5.6}$$

where R_T is the midband value of Z_T. By integrating (5.6) up to 61 GHz ($2f_{3\text{-}dB}$), the simulated $i_{n,in}^{rms}$ is 9.7 μA. A corresponding averaged noise current density of 55.7

pA/√Hz can be obtained from $i_{n,in}^{rms}/\sqrt{f_{3\text{-}dB}}$, and the estimated sensitivity of the proposed TIA is 135.8 μA for a bit error rate (BER) of 10^{-12}. The comparison of the averaged noise current density with other 40-Gb/s TIAs is shown in Table 5.1 [60]-[61]. In the proposed TIA, the gain of the first stage is somewhat small (~ 3.5 dB) resulting in a higher noise level when referred back to the input. The thermal noise generated from R_{M1} and R_{M2} which are optimized for wideband matching to a 50-Ω source termination is also a contributor to the input noise current.

Ref.	This work	[62]	[63]	[64]	[65]	[60]	[61]	[66]
BW (GHz)	30.5	30	9.2	8	7.2	42	47	50
Speed (Gb/s)	40	40	10	10	10	40	40	40
Z_T (dBΩ)	51	48	54	53	61	59	50	43
Z_{IN} (Ω)	54	—	—	—	—	35	—	79*
S_{22} (dB)	-10	—	—	—	—	-8	-10	-12
Noise (pA/√Hz)	55.7 (sim.)	—	16.7 (sim.)	18	8.2	34.2	29	—
C_{pd} (fF)	50	—	500	250	250	—	—	—
Chip area (mm^2)	1.17 × 0.46	0.8 × 1.3	0.8 × 0.8	0.6 × 0.6	0.14	1 × 1	0.675 × 0.975	0.78 × 1.18
V_{DD} (V)	1.8	1.8	2.5	1.8	1.8	5.2	5.2	5.2
P_{DC} (mW)	60.1	50.4	137.5	13.5	70.2	600	458	182
GBW/P_{DC} (GHzΩ/mW)	180.1	149.5	33.5	264.7	115.1	62.4	64.7	38.8
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm Bi-CMOS	0.18-μm CMOS	0.18-μm CMOS	SHBT f_T= 150GHz	DHBT f_T= 160GHz	SiGe f_T= 200GHz

* In the paper, S_{11}, S_{21}, and Z_T are -13 dB, 6.5 dB, and 43 dBΩ, respectively. The calculated Z_{IN} is 79 Ω.

Table 5.1. TIA Performance summary and comparison with other works.

With a 1.8 V supply voltage, the amplifier consumes 60.1 mW, and a

gain-bandwidth product per DC power figure-of-merit (GBW/P_{dc}) of 180.1 GHzΩ/mW is obtained. The circuit performance of the 40-Gb/s TIA is summarized in Table 5.1 together with four state-of-the-art 0.18-μm CMOS TIAs [62]-[65] and three 40-Gb/s TIAs using SiGe and III-V technologies [60]-[61], [66] published recently. As can be seen, the proposed TIA is comparable with those using the technologies with much higher f_T [60]-[61], [64].

5.4 Measured Transient Responses

To measure the transient response of the 40-Gb/s TIA, a 2^{31}-1 PRBS is applied. The high-speed PRBS is generated from the multiplexer MP1803A using the 4-data-output pattern generator MP1758A, and synchronized by the signal generator MG3695B. With an input current swing of 740 μA_{pp}, the output eye diagrams at 10-, 20-, 30-, and 40-Gb/s are shown in Fig. 5.12 with an output voltage swing of 263 mV_{pp}.

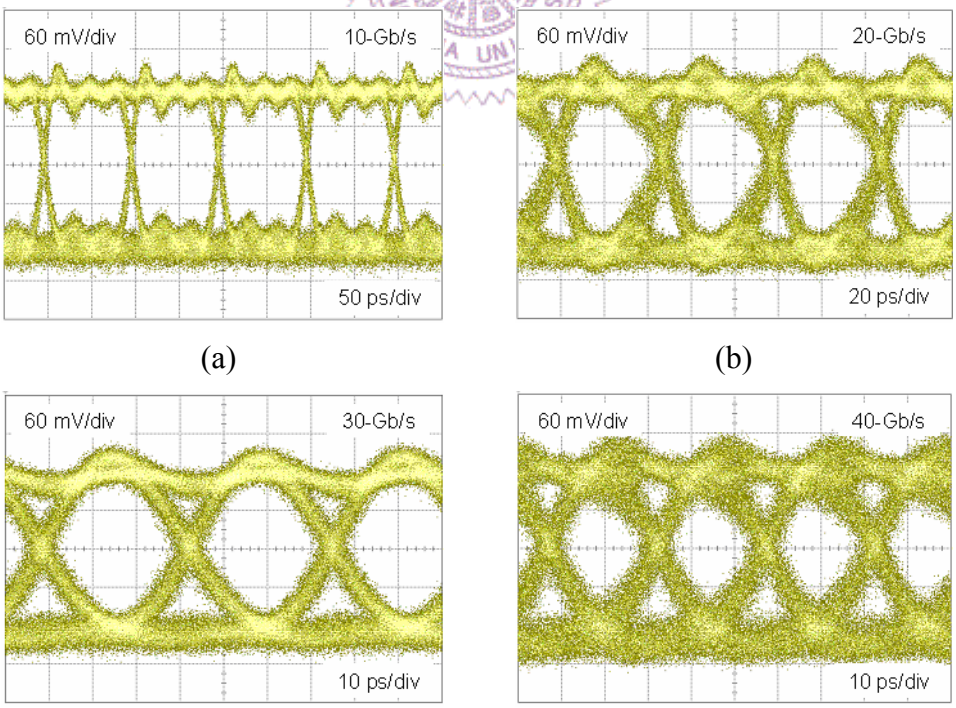


Fig. 5.12. Measure eye-diagram with a 2^{31}-1 PRBS input current of 740 μA_{pp} at (a) 10-Gb/s, (b) 20-Gb/s, (c) 30-Gb/s, and (d) 40-Gb/s.

5.5 Summary

An effective bandwidth improvement technique, PIP, has been demonstrated by a 0.18-μm CMOS TIA. Analyses about the noise current characteristics in the PIP configuration were also provided. From the measured results, the proposed circuit presents a circuit bandwidth of 30.5 GHz and a GBW/P_{dc} up to 180.1 GHzΩ/mW

Chapter VI: Conclusions and Future Work

In this dissertation, a fully-integrated CMOS BA was presented, and demonstrated a gain of 45.0 dB at around 24 GHz with an unconditional stability. The input and output ports were both matched well. Under a supply voltage of 1 V, *NF* and $P_{1dB,\ out}$ were 10.8 dB and -2.3 dBm, respectively. With the proposed PPR design technique and the employment of the lumped-element couplers, the proposed BA showed the highest $G_p f_p / P_{DC}$ figure-of-merit of 34.3 GHz/mW among the published results.

For the broadband application, an effective bandwidth improvement technique PIP has been demonstrated by a 0.18-μm CMOS TIA. The PIP technique can enhance the bandwidth of a cascaded CS stage by a factor of 3.31. The design concept was discussed in detail and the related equations were derived. Analyses about the noise current characteristics in the PIP configuration were also provided. From the measured results, the proposed circuit presents a circuit bandwidth of 30.5 GHz and a GBP/P_{dc} of 180.1 GHzΩ/mW.

6.1 Future Work

The successfully demonstrated design techniques for enhancing the CMOS integrated amplifiers at microwave frequencies enable further studies for various applications. The PPR technique can be implanted for different RF building blocks such as mixers, oscillators, power amplifiers, and synthesizer etc. The PIP technique can also be utilized for high-speed building blocks for wideband applications such as limiting amplifier, laser/modulator driver, clock and data recovery, multiplexer, and de-multiplexer.

References

[1] W. R. Deal, M. Biedenbender, P. Liu, J. Uyeda, and M. Siddiqui *et al.*, "Design and analysis of broadband dual-gate balanced low-noise amplifiers," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2107-2115, Oct. 2007.

[2] M. A. Masud, H. Zirath, and M. Kelly, "A 45-dB variable-gain low-noise MMIC amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 6, pp. 2848-2855, June 2006.

[3] J. Wang, X. Zhu, and D. Pavlidis, "Low-power InP/GaAsSb/InP DHBT cascade transimpedance amplifier with GBP/Pdc of 7.2 GHz/mW," *Electron. Lett.*, vol. 42, no. 1, pp. 25-27, Jan. 2006.

[4] E. Kerherve, C. P. Moreira, P. Jarry, and L. Courcelle, "40-Gb/s wide-band MMIC pHEMT modulator driver amplifiers designed with the real frequency technique," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 6, pp. 2145-2152, June 2005.

[5] S. Masuda, T. Takahashi, and K. Joshin, "An over-110-GHz InP HEMT flip-chip distributed baseband amplifier with inverted microstrip line structure for optical transmission system," *IEEE J. Solid-State Circuits*, vol. 38, no. 9, pp. 1479-1484, Sept. 2003.

[6] B. A. Floyd, "V-band and W-band SiGe bipolar low-noise amplifiers and voltage-controlled oscillators," in *IEEE RFIC Symp. Dig.*, June 2004, pp. 295-298.

[7] N. Tanzi, J. Dykstra, and K. Hutchinson, "A 1-watt doubly balanced 5GHz flip-chip SiGe power amplifier," in *IEEE RFIC Symp. Dig.*, June 2003, pp. 141-144.

[8] A. Schild, H.-M. Rein, J. Mullrich, L. Altenhain, and J. Blank *et al.*, "High-gain SiGe transimpedance amplifier arry for a 12 × 10 Gb/s parallel optical-fiber link," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 4-12, Jan. 2003.

[9] S. Mandegaran and A. Hajimiri, "A breakdown voltage multiplier for high voltage swing drivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 302-312, Feb. 2007.

[10] Q. He and M. Feng, "Low-power, high-gain, and high-linearity SiGe BiCMOS wide-band low-noise amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 956-959, June 2004.

[11] E. Morifuji, and H. S. Momose, T. Ohguro, T. Yoshitomi, and H. Kimijima *et al.*, "Future perspective and scaling down roadmap for RF CMOS," in *IEEE VLSI Circuits Symp. Dig. Tech. Papers*, June 1999, pp. 165-166.

[12] W. Wu, S. Lam, and M. Chan, "Effects of layout methods of RF CMOS on noise

performance," *IEEE Trans. Electron Devices*, vol. 52, no. 12, pp. 2753-2759, Dec. 2005.

[13] N. Zhang, C.-M. Hung, and K. K. O, "80-GHz tuned amplifier in bulk CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 2, pp. 121-123, Feb. 2008.

[14] B. A. Floyd, L. Shi, Y. Taur, I. Lagnado, and K. K. O, "A 23.8-GHz SOI CMOS tuned amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 9, pp. 2193-2196, Sept. 2002.

[15] Y.-C. Ho, K.-H. Kim, B. A. Floyd, C. Wann, and Y. Taur *et al.*, "4- and 13-GHz tuned amplifiers implemented in a 0.1-μm CMOS technology on SOI, SOS, and bulk substrates," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2066-2073, Dec. 1998.

[16] D. J. Cassan and J. R. Long, "A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LNA in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 427-435, Mar. 2003.

[17] J.-D. Jin and S. S. H. Hsu, "A 0.18-μm CMOS balanced amplifier for 24-GHz applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 440-445, Feb. 2008.

[18] J.-D. Jin and S. S. H. Hsu, "A 1-V, 45-GHz balanced amplifier with 21.5-dB gain using 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 3, pp. 599-603, Mar. 2008.

[19] S. Galal and B. Razavi, "10-Gb/s limiting amplifier and laser/modulator driver in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2138-2146, Dec. 2003.

[20] J. A. Mataya, G. W. Haines, and S. B. Marshall, "IF amplifier using C_c compensated transistors," *IEEE J. Solid-State Circuits*, vol. SC-3, no. 4, pp. 401-407, Dec. 1968.

[21] A. Arbabian and A. M. Niknejad, "A broadband distributed amplifier with internal feedback providing 660GHz GBW in 90nm CMOS," in *IEEE ISSCC Dig. Tech. Paper*, Feb. 2008, pp. 196-197.

[22] J.-C. Chien and L.-H. Lu, "40Gb/s high-gain distributed amplifiers with cascaded gain stages in 0.18μm CMOS," in *IEEE ISSCC Dig. Tech. Paper*, Feb. 2007, pp. 538-539.

[23] R.-C. Liu, T.-P. Wang, L.-H. Lu, H. Wang, and S.-H. Wang *et al.*, "An 80GHz traveling-wave amplifier in a 90nm CMOS technology," in *IEEE ISSCC Dig. Tech. Paper*, Feb. 2005, pp. 154-155.

[24] J. Kim, J.-O. Plouchart, N. Zamdmer, R. Trzcenski, and R. Groves *et al.*, "A 12dBm 320GHz GBW distributed amplifier in a 0.12μm SOI CMOS," in *IEEE ISSCC Dig. Tech. Paper*, Feb. 2004, pp. 478-479.

[25] B. Kleveland, C. H. Diaz, D. Vook, L. Madden, and T. H. Lee *et al.*, "Monolithic CMOS distributed amplifier and oscillator," in *IEEE ISSCC Dig. Tech. Paper*, Feb. 1999, pp. 70-71.

[26] S. S. Mohan, M. del M. Hershenson, S. P. Boyd, and T. H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 346-355, Mar. 2000.

[27] S. Galal and B. Razavi, "Broadband ESD protection circuits in CMOS

technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2334-2340, Dec. 2003.

[28] S. Galal and B. Razavi, "40-Gb/s amplifier and ESD protection circuit in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2389-2396, Dec. 2004.

[29] J.-D. Jin and S. S. H. Hsu, "40-Gb/s transimpedance amplifier in 0.18-μm CMOS technology," in *Proc. Eur. Solid-State Circuits Conf.*, Sept. 2006, pp. 520-523.

[30] J.-D. Jin and S. S. H. Hsu, "A 40-Gb/s transimpedance amplifier in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1449-1457, June 2008.

[31] S. Shekhar, J. S. Walling, and D. J. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2424-2439, Nov. 2006.

[32] J.-D. Jin and S. S. H. Hsu, "A 70-GHz transformer-peaking broadband amplifier in 0.13-μm CMOS technology," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2008, pp. 285-288.

[33] C.-F. Liao and S.-I. Liu, "40 Gb/s transimpedance-AGC amplifier and CDR circuit for broadband data receivers in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 642-655, Mar. 2008.

[34] J.-D. Jin and S. S. H. Hsu, "Wideband CMOS transimpedance amplifier design using transformer-peaking technique," in *Solid State Devices and Materials*, Sept. 2007, pp. 492-493.

[35] TSMC, *TSMC 0.18μm mixed signal 1P6M salicide 1.8V/3.3V RF spice models*, T-018-MM-SP-001, Sept. 2004.

[36] S. F. Tin, A. A. Osman, K. Mayaram, and C. Hu, "A simple subcircuit extension of the BSIM3v3 model for CMOS RF design," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 612-624, Apr. 2000.

[37] M. S. Gupta, "Power gain in feedback amplifiers, a classic revisited," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 5, pp. 864-879, May 1992.

[38] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge, U.K.: Cambridge Univ. Press, 2004.

[39] Sonnet. Sonnet Softw., North Syracuse, NY, 2003. [Online]. Available: http://www.sonnetusa.com

[40] R. S. Engelbrecht and K. Kurokawa, "A wideband low noise L-band balanced transistor amplifier," *Proc. IEEE*, vol. 53, no. 3, pp. 237-247, Mar. 1965.

[41] K. Kurokawa, "Design theory of balanced transistor amplifiers," *Bell Syst. Tech. J.*, vol. 44, pp. 1675-1698, Oct. 1965.

[42] I. Bahl, Lumped Elements for RF and Microwave Circuits. Norwood, MA: Artech House, 2003.

[43] R. C. Frye, S. Kapur, and R. C. Melville, "A 2-GHz quadrature hybrid

implemented in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 550-555, Mar. 2003.

[44] J.-D. Jin, S. S. H. Hsu, M.-T. Yang, and S. Liu, "Low-loss differential semicoaxial interconnects in CMOS process," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4333-4340, Dec. 2006.

[45] A. Komijani, A. Natarajan, and A. Hajimiri, "A 24-GHz, +14.5-dBm fully integrated power amplifier in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1901-1908, Sep. 2005.

[46] G. Ghione and C. Naldi, "Parameters of coplanar waveguides with lower ground plane," *Electron. Lett.*, vol. 19, no. 18, pp. 734-735, Sep. 1983.

[47] J.-D. Jin, S. S. H. Hsu, M.-T. Yang, and S. Liu, "Low-loss single and differential semi-coaxial interconnects in standard CMOS process," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2006, pp. 420-423.

[48] M. T. Yang, P. P. C. Ho, T. J. Yeh, Y. J. Wang, and D. C. W. Kuo et al., "On the millimeter-wave characteristics and model of on-chip interconnect transmission lines up to 110 GHz," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2005, pp. 1819-1822.

[49] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 1997.

[50] Agilent. *Using Advanced Design System to Design an MMIC Amplifier*, Application Note Number 1462. [Online]. Available: http://literature.agilent.com/litweb/pdf/5988-9637EN.pdf

[51] X. Guan and A. Hajimiri, "A 24-GHz CMOS front-end," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 368-373, Feb. 2004.

[52] L. M. Franca-Neto, B. A. Bloechel, and K. Soumyanath, "17 GHz and 24 GHz LNA designs based on extended-S-parameter with microstrip-on-die in 0.18 μm logic CMOS technology," in *Proc. Eur. Solid-State Circuits Conf.*, Sep. 2003, pp. 149-152.

[53] K.-W. Yu, Y.-L. Lu, D.-C. Chang, V. Liang, and M. F. Chang, "K-band low-noise amplifiers using 0.18 μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 14, no. 3, pp. 106-108, Mar. 2004.

[54] B. Razavi, *Design of Integrated Circuits For Optical Communications*. Singapore: McGraw-Hill, 2003.

[55] http://www.u2t.de/

[56] K. Han, J. Gil, S.-S. Song, J. Han, and H. Shin *et al.*, "Complete high frequency thermal noise modeling of short-channel MOSFETs and design of 5.2-GHz low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 726-735, Mar. 2005.

[57] K. Han, H. Shin, and K. Lee, "Analytical drain thermal noise current model valid for deep submicron MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 261-269, Feb. 2004.

[58] C. Kromer, G. Sialm, T. Morf, M. L. Schmatz, and F. Ellinger *et al.*, "A low-power 20-GHz 52-dBΩ transimpedance amplifier in 80-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 885-894, June 2004.

[59] E. Sackinger, *Broadband Circuits For Optical Fiber Communication*. New York: Wiley, 2005.

[60] C. Q. Wu, E. A. Sovero, and B. Massey, "40-GHz transimpedance amplifier with differential outputs using InP-InGaAs heterojunction bipolar transistors," *IEEE J. Solid-State Circuits*, vol. 38, no. 9, pp. 1518-1523, Sep. 2003.

[61] J. S. Weiner, J. S. Lee, A. Leven, Y. Baeyens, and V. Houtsma *et al.*, "An InGaAs-InP HBT differential transimpedance amplifier with 47-GHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 10, pp. 1720-1723, Oct. 2004.

[62] R.-C. Liu and H. Wang, "DC-to-15- and dc-to-30-GHz CMOS distributed transimpedance amplifiers," in *IEEE RFIC Symp. Dig. Papers*, June 2004, pp. 535-538.

[63] B. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, no. 8, pp. 1263-1270, Aug. 2004.

[64] Z. Lu, K. S. Yeo, J. Ma, M. A. Do, W. M. Lim, and X. Chen, "Broadband design techniques for transimpedance amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 3, pp. 590-600, Mar. 2007.

[65] C.-H. Wu, C.-H. Lee, W.-S. Chen, and S.-I. Liu, "CMOS wideband amplifiers using multiple inductive-series peaking technique," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 548-552, Feb. 2005.

[66] J. S.Weiner, A. Leven, V. Houtsma, Y. Baeyens, and Y.-K. Chen *et al.*, "SiGe differential transimpedance amplifier with 50-GHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 38, no. 9, pp. 1512-1517, Sep. 2003.

Vita

Research Interests: High-speed and low-noise integrated circuits and device modeling applied to the areas of wireline/wireless communications and bioelectronics.

Education:

2003-2008	National Tsing Hua University, Hinchu, Taiwan Doctor of Philosophy in Electronics Engineering
2001-2003	National Tsing Hua University, Hinchu, Taiwan Master of Science in Electronics Engineering
1999-2001	Kun Shan University, Tainan, Taiwan Bachelor of Science in Electronics Engineering
1994-1999	Tung Nan Institute of Technology, Taipei, Taiwan Associate Bachelor of Science in Electronics Engineering

Academic Experience:

2008/03-2008/11	Visiting Scholar Purdue University, West Lafayette, Indiana USA

Industrial Experience:

2006/10-2008/02	Intern TSMC, Hsinchu, Taiwan
2004/06-2004/09	Summer Intern TSMC, Hsinchu, Taiwan

Competition Experiences:

日期	比賽名稱	主辦單位	成積
2001/03	義隆盃單晶片微控制器應用製作大賽	義隆電子	特優
2001/12	影像伺服即時追蹤控制應用	教育部顧問室伺服電機工業教學資源中心	團隊創意獎
2003/01	台灣區溫度感應器設計大賽	美國國家半導體	亞軍
2006/07	TSMC Outstanding Student Research Award	台灣積體電路	第三名
2007/05	晶片製作成果發表會	國家晶片系統設計中心	特別設計獎
2007/05	晶片製作成果發表會	國家晶片系統設計中心	佳作設計獎
2007/07	7th 旺宏金矽獎	旺宏電子	評審團鑽石大賞
2007/12	補助博士生赴國外研究	國科會	入選
2008/05	晶片製作成果發表會	國家晶片系統設計中心	優良設計獎
2008/07	8th 旺宏金矽獎	旺宏電子	優勝獎
2008/11	科技研究獎學金	中技社	入選

Publication List

Journal papers:

[1] **Jun-De Jin**, Shawn S. H. Hsu, Ming-Ta Yang, and Sally Liu, "Low-loss differential semicoaxial interconnects in CMOS process," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4333-4340, Dec. 2006.

[2] Yi-Jing Lin, Shawn S. H. Hsu, **Jun-De Jin**, and C. Y. Chan, "A 3.1-10.6 GHz ultra-wideband CMOS low noise amplifier with current-reused technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 3, pp. 232-234, Mar. 2007.

[3] Hong-Yu Lin, Shawn S. H. Hsu, Chih-Yuan Chan, **Jun-De Jin**, and Yu-Syuan Lin, "A wide locking-range frequency divider for LMDS applications," *IEEE Trans. Circuits and Systems II*, vol. 54, no. 9, pp. 750-754, Sept. 2007.

[4] **Jun-De Jin** and Shawn S. H. Hsu, "A 0.18-μm CMOS balanced amplifier for 24-GHz applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 440-445, Feb. 2008.

[5] **Jun-De Jin** and Shawn S. H. Hsu, "A 1-V, 45-GHz balanced amplifier with 21.5-dB gain using 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 3, pp. 599-603, Mar. 2008.

[6] **Jun-De Jin**, Shawn S. H. Hsu, Tzu-Jin Yeh, Ming-Ta Yang, and Sally Liu, "Fully analytical modeling of Cu interconnects up to 110 GHz," *Jpn. J. Appl. Phys.*, vol. 47, no. 4, pp. 2473-2476, Apr. 2008.

[7] **Jun-De Jin** and Shawn S. H. Hsu, "A 40-Gb/s transimpedance amplifier in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1449-1457, June 2008.

[8] **Jun-De Jin** and Shawn S. H. Hsu, "A miniaturized 70-GHz broadband amplifier in 0.13-μm CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 12, pp. 3086-3092, Dec. 2008.

[9] **Jun-De Jin** and Shawn S. H. Hsu, "A 75-dBΩ 10-Gb/s transimpedance amplifier in 0.18-μm CMOS technology," *IEEE Photon. Technol. Lett.*, vol. 20, no. 24, pp. 2177-2179, Dec. 2008.

[10] Y. Wei, S. Hsu, and **Jun-De Jin**, "A low-power low-noise amplifier for K-band applications," *IEEE Microw. Wireless Compon. Lett.*, to be published.

Conference papers:

[1] Kuo-Chin Hsueh, **Jun-De Jin**, Yen-Han Lai, and Long-Sheng Fan, "A linear magnetic tweezers for precise particle manipulations," *The 2nd International Symposium on Micro & Nano Technology*, Mar. 2006.

[2] **Jun-De Jin**, Shawn S. H. Hsu, Ming-Ta Yang, and Sally Liu, "Low-loss single and differential semi-coaxial interconnects in standard CMOS process," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2006, pp. 420-423.

[3] **Jun-De Jin** and Shawn S. H. Hsu, "40-Gb/s transimpedance amplifier in 0.18-μm CMOS technology," in *Proc. Eur. Solid-State Circuits Conf.*, Sept. 2006, pp. 520-523.

[4] Chih-Yuan Chan, **Jun-De Jin**, Yu-Syuan Lin, Shawn S. H. Hsu, and Ying-Zong Juang, "STI effect on flicker noise in 0.13-μm RF NMOS," in *Proc. Eur. Solid-State Device Research Conf.*, Sept. 2006, pp. 101-104.

[5] Long-Sheng Fan, Shawn S. H. Hsu, **Jun-De Jin**, Cheng-Yu Hsieh, Wei-Chen Lin, H. C. Hao, Hsin-Li Cheng, Kuo-Chih Hsueh, and Chen-Zong Lee, "Miniaturization of magnetic resonance microsystem components for 3D cell imaging," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2007, pp. 166-167.

[6] **Jun-De Jin** and Shawn S. H. Hsu, "Wideband CMOS transimpedance amplifier design using transformer-peaking technique," in *Solid State Devices and Materials*, Sept. 2007, pp. 492-493.

[7] **Jun-De Jin**, Shawn S. H. Hsu, Tzu-Jin Yeh, Ming-Ta Yang, and Sally Liu, "Fully analytical modeling of Cu interconnects up to 110 GHz," in *Solid State Devices and Materials*, Sept. 2007, pp. 908-909.

[8] **Jun-De Jin** and Shawn S. H. Hsu, "A 70-GHz transformer-peaking broadband amplifier in 0.13-μm CMOS technology," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2008, pp. 285-288.