A 70-GHz Transformer-Peaking Broadband Amplifier in 0.13-μm CMOS Technology

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***Abstract* — A 70-GHz broadband amplifier is realized in a 0.13-μm CMOS technology. By using five cascaded common-source stages with the proposed asymmetric transformer peaking technique, the measured bandwidth and gain can reach 70.6 GHz and 10.3 dB respectively under a power consumption (P_{DC}) of 79.5 mW. With miniaturized transformer design, the core area of the circuit is only ~ 0.05 mm^2. Compared with the state-of-the-art CMOS broadband amplifiers, this work achieves the highest gain-bandwidth product (*GBW*) of 231 GHz and also the highest GBW/P_{DC} of 2.9 GHz/mW.**

***Index Terms* — Broadband amplifier, CMOS, common-source stage, gain-bandwidth product, transformer peaking.**

I. Introduction

The millimeter-wave broadband amplifier is one of the key circuit blocks for high-speed optical communication systems. For wideband applications, previously reported results were mostly fabricated in III-V [1]-[3] or SiGe [4]-[5] technologies to gain the better transistor performance. However, owing to the rapid scaling in the feature size, CMOS technology also becomes an excellent candidate for such applications. Not only with comparable f_T and f_{max}, but the MOS transistor also features high integration level, high yield, low power consumption, and low cost. Recent advances successfully demonstrated several wideband amplifiers using CMOS technologies [6]-[14].

Two design approaches are commonly adopted for wideband amplifiers in these studies, namely, the distributed amplifier (DA) topology [1]-[3], [6]-[10] and the inductive peaking technique [11]-[14]. The disadvantages of the DA topology are the relatively large power consumption and chip area due to the long length and the associated loss of the transmission lines. On the other hand, the circuit area is mainly limited by the size of the inductive components if using the inductive peaking technique.

In this study, a 0.13-μm CMOS broadband amplifier is realized using the proposed asymmetric transformer peaking technique in a simple cascaded common-source (CS) configuration. By an effective frequency peaking design using transformers, this work achieves a bandwidth of 70.6 GHz under a low power consumption of 79.5 mW. The miniaturized transformers using the interconnect layers in the CMOS process result in an overall circuit core area of only ~ 0.05 mm^2.

II. Design of Broadband Amplifier

The circuit topology of the proposed broadband amplifier is shown in Fig. 1. Transformers with a positive coupling coefficient k are employed to extend the operation frequency and also for input/output impedance matching. One zero and two pairs of complex conjugate poles are introduced by the transformers at different frequencies to enhance the circuit bandwidth. A shunt resistor R_M is placed at the input node together with the input transformer for impedance matching. A similar topology is also employed in the last stage for output matching using the drain bias resistor R_D. For low voltage and low power operation, the simple CS design is adopted instead of the typically used cascode topology for RF applications. As shown in the figure, five stages are cascaded to provide a high gain amplification while still maintaining an overall low power consumption.

Fig. 2 compares the simulated results by applying various peaking techniques to the identical basic configuration of a five-stage CS design. Based on the foundry provided BSIM model and the ideal inductive components, these designs present a similar low-frequency gain but with an obvious bandwidth difference. Without using any inductive peaking techniques, the low-frequency gain is 10.3 dB and the circuit bandwidth is only 7.0 GHz, as shown in Fig. 2, curve *A*. With the proposed asymmetric transformer peaking technique, a bandwidth up to 81.4 GHz (increased by ~ 11.6×) can be achieved as indicated by curve *F*.

The most straightforward wideband technique is the shunt inductor peaking [11]. By placing an inductor in series with the load resistor R_D, the drain capacitance C_d and the gate capacitance C_g of the next stage can be canceled out by the shunt *LC* resonance. As a result, the bandwidth is increased up to 34.1 GHz, as shown by curve *B*. For curve *C*, one more inductor is connected in series between the drain and the gate of the next stage to form the shunt-series peaking [12], and the bandwidth can be further enhanced to 55.5 GHz.

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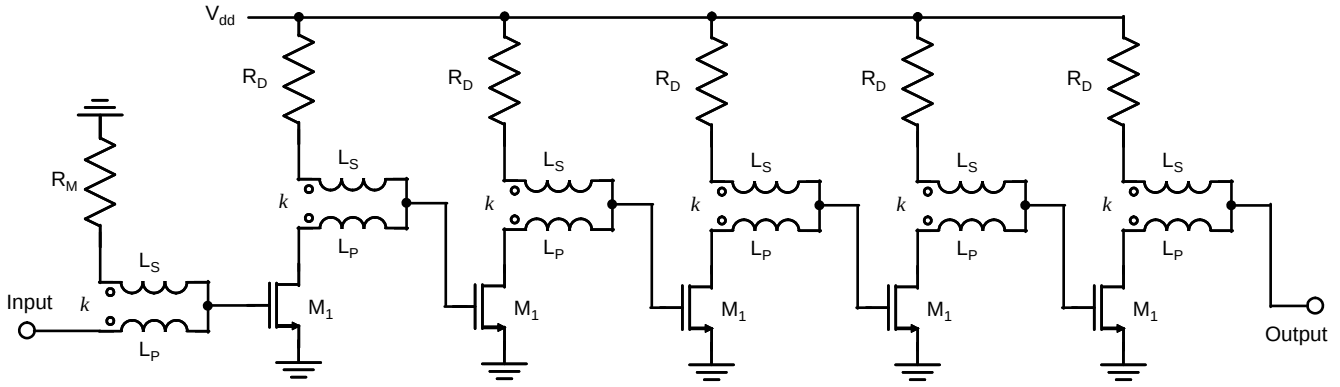

Fig. 1. Circuit topology of the CMOS broadband amplifier.

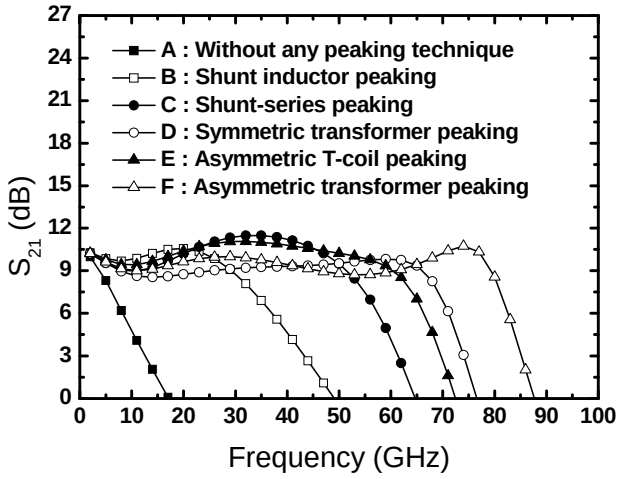

Fig. 2. Simulated frequency responses with different inductive peaking techniques.

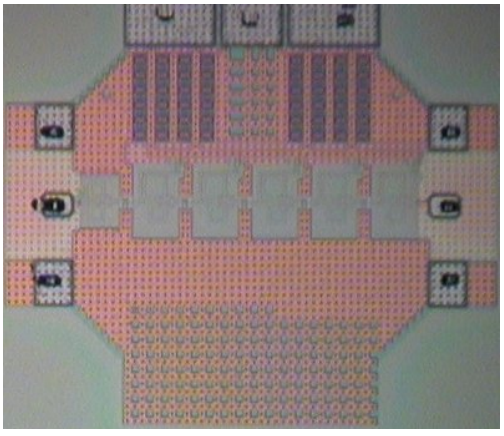

Fig. 3. Chip photograph. (Chip area: 0.66 × 0.59 mm^2, core area: 0.48 × 0.11 mm^2).

As shown by curve *D*, the symmetric transformer peaking technique is employed [13], which has a positive k and the identical primary coil L_P and secondary coil L_S inductances in each transformer. Similar to the proposed asymmetric transformer peaking design, one zero and two pairs of complex poles are also introduced. However, the bandwidth is enhanced to only 69.7 GHz since the identical L_P and L_S resulting in lower pole/zero frequencies. The result of a recently published peaking technique, asymmetric T-coil peaking [14], is shown by curve *E*, where k is negative and L_P and L_S are different. As can be seen, the obtained bandwidth of the amplifier with asymmetric T-coil peaking is 64.7 GHz. With the asymmetric T-coil design, the unequaled inductances can accommodate the unequaled parasitic loading capacitances for an enhanced bandwidth extension. However, with a negative k, the impedance looking into L_P is large, which reduces the current $g_m v_{gs}$ flowing into the gate capacitance C_g and handicaps the bandwidth enhancement. By using asymmetric transformer peaking with a positive k, a simulated circuit bandwidth of 81.4 GHz can be achieved, as shown by curve *F*.

III. Measurement Results

The broadband amplifier was fabricated in a standard 1P8M 0.13-μm CMOS process. The chip area including the DC and RF probing pads is 0.66 × 0.59 mm^2, while the core area is only 0.48 × 0.11 mm^2 (~ 0.05 mm^2), as shown in Fig. 3. The on-wafer S-parameters measurement was performed from 2 GHz to 100 GHz. The measured S_{21} at low frequencies is 10.3 dB and the circuit bandwidth is 70.6 GHz under a power consumption P_{DC} of 79.5 mW, as shown in Fig. 4. The measured maximum S_{11} and S_{22} are -6.1 dB and -10.8 dB within the circuit bandwidth, as shown in Fig. 5 and 6, respectively. The reverse isolation S_{12} is well below -30 dB up to 100 GHz, as shown in Fig. 7.

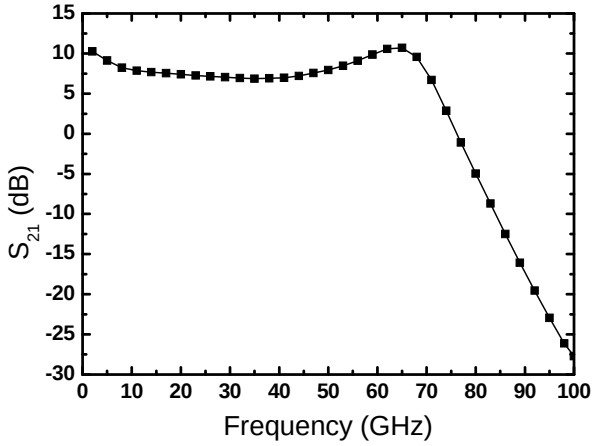

Fig. 4. Measured S_{21} of the proposed broadband amplifier.

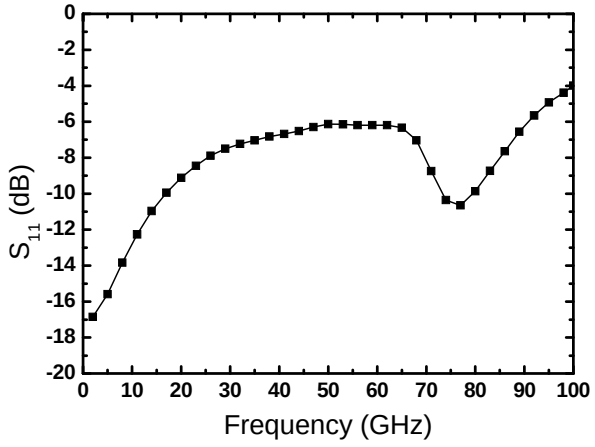

Fig. 5. Measured S_{11} of the proposed broadband amplifier.

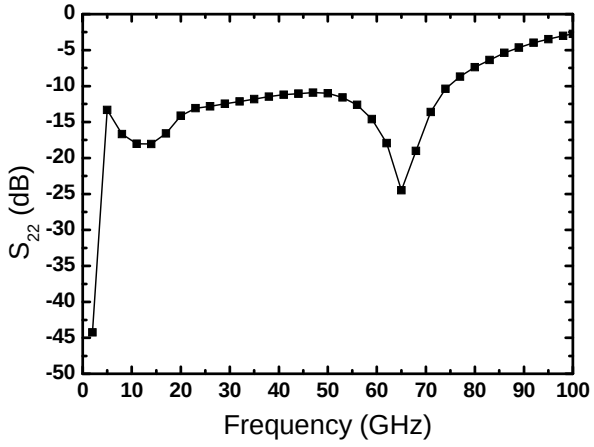

Fig. 6. Measured S_{22} of the proposed broadband amplifier.

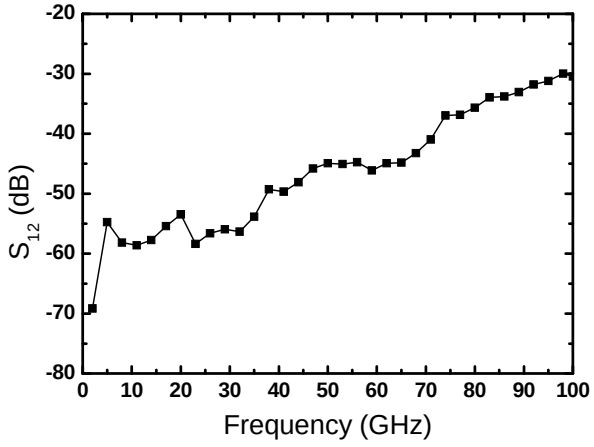

Fig. 7. Measured S_{12} of the proposed broadband amplifier.

Compared to the state-of-the-art CMOS broadband amplifiers [6]-[10], this work achieves the highest gain-bandwidth product (*GBW*) of 231 GHz and the highest GBW/P_{DC} of 2.9 GHz/mW. In addition, the core area is only ~ 0.05 mm^2, which is also the smallest one compared with other works.

IV. Conclusion

A 10-dB 70-GHz broadband amplifier was successfully demonstrated in a standard 0.13-μm CMOS technology. By using the proposed asymmetric transformer peaking technique together with a simple CS cascaded design, the amplifier achieved the highest *GBW* and GBW/P_{DC} figure-of-merits among the published CMOS broadband amplifiers. The core circuit of this design only occupied a chip area of ~ 0.05 mm^2.

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