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Fully Analytical Modeling of Cu Interconnects Up to 110 GHz

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1. Introduction

The operation frequency of the integrated-circuits using advanced CMOS technology has been exceeded 100 GHz [1]. One important role is the copper (Cu) interconnects because the impact on circuit characteristics can no longer be neglected. However, the modeling and the characteristics of the Cu interconnects up to such a high frequency has not been reported.

Various interconnects modeling approaches has been reported [2]-[5]. An analytical approach has been used by considering only part of the high-frequency effects and is verified up to relative low frequencies [2]. In addition, semi-empirical models were employed for better agreement between the measured and modeled results [3]-[5]. In this study, a simple approach with multi-section *RLGC* elements, but fully physical-based and scalable, is proposed and verified up to 110 GHz. Additionally, the Cu interconnects with and without Si-substrate shielding are studied. Compared with the shielded cases, unshielded interconnect model needs to take into account the effects introduced by the lossy Si substrate.

2. Modeling of Interconnects

The Cu interconnects are fabricated using a standard 0.13-μm CMOS process which provides eight metal layers for a flexible interconnect design. The signal line is realized by metal eight (M8), with a width and a thickness of 2.5 μm (w_s) and 3.3 μm (t_s), respectively. The Si substrate shielding is realized by M1 with a thickness of 0.28 μm (t_g). A silicon dioxide (SiO_2) layer with a thickness of 6.3 μm (t_{ox}) and an equivalent dielectric constant (ε_r) of 4.04 is used between M8 and M1, while a thickness of 7.07 μm (t_{ox1}) and an equivalent ε_r of 4.05 is employed between M8 and the Si substrate.

Modeling of the Cu interconnects is based on the distributed *RLGC* circuit model, due to the advantages of a simple yet physical-based circuit topology, as shown in Fig. 1. Each component in the model, as shown in the following, is calculated based on their physical characteristics. In addition, it was found that the interconnects with a length of 1000 μm can be modeled precisely by only 20 *RLGC* sections. The calculation of each component in the distributed interconnect model for both with (denoted as $R_{w\text{-}s}$, $L_{w\text{-}s}$, $G_{w\text{-}s}$, and $C_{w\text{-}s}$) and without (denoted as $R_{wo\text{-}s}$, $L_{wo\text{-}s}$, $G_{wo\text{-}s}$, and $C_{wo\text{-}s}$) substrate shielding are described as follows.

Cu Interconnects with Substrate Shielding

In this case, $R_{w\text{-}s}$ is the sum of DC resistance and the

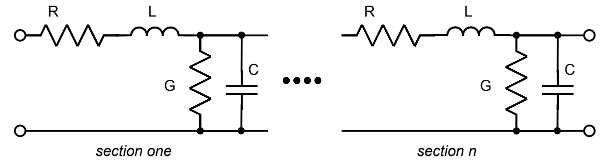

Fig. 1 A typical distributed *RLGC* equivalent circuit with *n* sections for interconnects.

AC resistance originated from the skin effect in the finite metal width and thickness of both the signal and ground lines [2]. The proximity effect was not taken into account since the skin effect dominates the reduction in current loop area at high frequencies. On the other hand, the calculation of $L_{w\text{-}s}$ considers both the skin and proximity effects, which can be described by a frequency-dependent internal inductance (L_{int}) and a frequency-independent external inductance (L_{ext}) [6]:

$$L_{\text{int}} = \frac{\mu_0}{2\pi}\frac{3}{8}\tanh\left(\frac{2\pi\delta_s}{w_s + t_s}\right) \quad (1)$$

$$L_{ext} = (\mu_0 / 2\pi)(2\ln[R_{12}] - \ln[r_1] - \ln[r_2]) \quad (2)$$

where

$$\ln[R_{12}] = \ln\left[100\left(\frac{2t_{ox} + t_s + t_g}{2}\right)\right] + k_1 \quad (3)$$

$$r_1 = 100 \times e^{-3/2}(w_s + t_s) \quad (4)$$

$$r_2 = 100 \times e^{-3/2}(w_g + t_g) \quad (5)$$

and where δ_s is the skin depth of the signal line and w_g is the ground line width. The $G_{w\text{-}s}$ and $C_{w\text{-}s}$ can be easily estimated by a parallel plate structure. With a frequency-dependent conductive loss, $G_{w\text{-}s}$ can be represented as:

$$G_{w-s} = \omega\varepsilon_r{}''\varepsilon_0 w_s / t_{ox} \quad (6)$$

where ε_r'' is the imaginary part of the dielectric constant of SiO_2. To calculate $C_{w\text{-}s}$, a geometry-dependent effective dielectric constant [2] and a fringing capacitance are both taken into account [7].

Cu Interconnects without Substrate Shielding

For the Cu interconnects without substrate shielding, the electromagnetic wave can penetrate into the lossy Si substrate, which is referred to as the substrate skin effect [8]. As a result, the series impedance (Z_{Si}) of the interconnects can be calculated as:

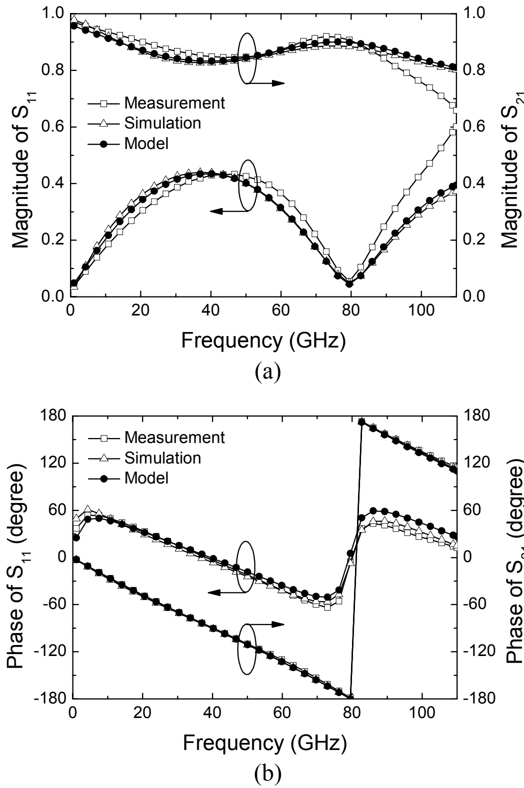

Fig. 2 (a) Magnitude and (b) phase of the measured, simulated, and modeled S-parameters of the Cu interconnect with substrate shielding. The length of the line is 1000 μm, and n is 20.

$$Z_{Si} = \frac{1}{\sigma_s w_s t_{ss}} + j\omega \frac{\mu_0}{2\pi} \ln\left[\frac{2t_{eq} + \delta_{Si} - j\delta_{Si}}{r_{eq}}\right] \quad (7)$$

where

$$t_{eq} = t_{ox1} + (t_{ss} - w_s)/4 \quad (8)$$

$$r_{eq} = (t_{ss} - w_s)/4 \quad (9)$$

$$t_{ss} = t_s \delta_s / (t_s + \delta_s) \quad (10)$$

and where σ_s is the conductivity of the signal line, δ_{Si} is the skin depth of the Si substrate.

In this case, $R_{wo\text{-}s}$ can be obtained from the real part of Z_{Si}, and $L_{wo\text{-}s}$ is the imaginary part of Z_{Si} divided by ω. As can be seen, $R_{wo\text{-}s}$ is determined not only by the metal signal line but also by the Si substrate. In addition, as a function of δ_{Si}, $L_{wo\text{-}s}$ presents a frequency-dependent characteristic. The $G_{wo\text{-}s}$ and $C_{wo\text{-}s}$ can be determined by a Si conductance and a Si capacitance first in a parallel connection, and then in series with a SiO_2 capacitance. These three are obtained based on the physical structure, and considered the geometry-dependent effective dielectric constants in a parallel plate structure.

3. Measured Results

The Cu interconnects were measured on-wafer from 1 to 110 GHz. Fig. 2 and Fig. 3 show the measured and modeled results for the interconnects with and without the substrate shielding, respectively. The simulated results from SONNET are also shown for comparison. For both types of Cu interconnects, as can be seen, the modeled S-parameters are in excellent agreement with the simulated and measured results in a wide frequency range.

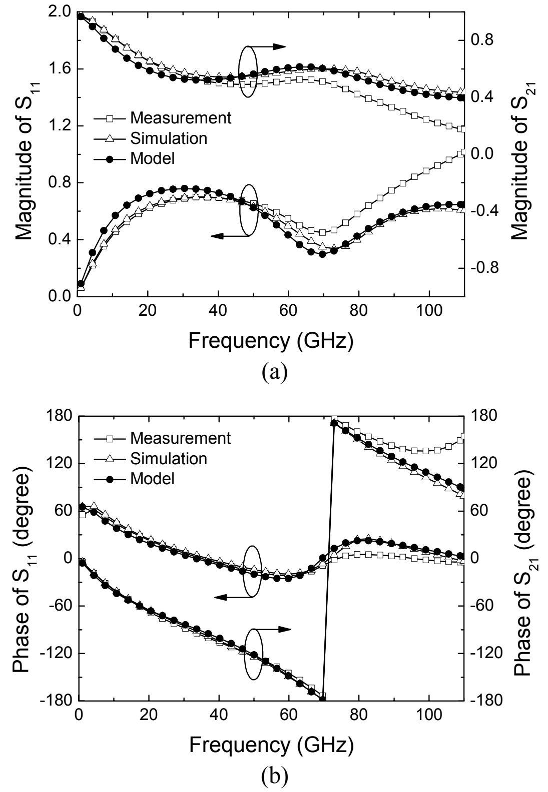

Fig. 3 (a) Magnitude and (b) phase of the measured, simulated, and modeled S-parameters of the Cu interconnect without substrate shielding.

4. Conclusions

A fully analytical approach with scalability for the Cu interconnects in a standard CMOS process was developed and verified up to 110 GHz. By carefully considering the frequency-dependent effects of each *RLGC* component, excellent agreement was observed between measured, modeled, and simulated S-parameters. The proposed simple approach is not only provided the physical insight but also showed excellent modeling accuracy for both shielded- and unshielded-type interconnects over a wide frequency range without any optimization procedure.

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