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Wideband CMOS Transimpedance Amplifier Design Using Transformer-Peaking Technique

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1. Introduction

The growing demands of communication capacity drive the optical communication data rate toward the Gb/s range. The design of front-end wideband transimpedance amplifiers (TIAs) is becoming more challenging for such applications. For wideband TIA design, inductor peaking technique can be used to increase the circuit bandwidth without sacrificing the low-frequency gain and the power consumption [1]-[3]. In this study, rather than the conventional approach, a novel technique of using transformer peaking has been employed. Consisting of two individual inductors and a mutual inductor, a transformer can increase the peaking effects and also reduce the chip area compared to the design with two individual inductors. Comparisons between circuits without peaking components, with inductor peaking, and with transformer peaking have been made. The results demonstrated the excellence of using the proposed approach.

2. Circuit Topology

The proposed TIA utilizes a cascade structure for large output swing and high gain under a low supply voltage of 1.8 V, as shown in Fig. 1. The input stage consists of a current source M_2 to bias a common-gate (CG) stage M_1, which provides impedance matching capability to the previous stage. M_1 also decouples the TIA and photodiode capacitance to minimize the impact of this capacitance on the circuit bandwidth [4]. The cascading common-source (CS) stages, M_3 and M_4, provide additional gain blocks to achieve a high gain performance. The feedback resistor R_f is used in the first CS stage to increase the bandwidth and stabilize the circuit. Output matching is realized by a resistor R_4 and a source follower M_5. The output matching stage also increases the isolation between the core circuit and the load. For bandwidth enhancement, the transformer TF_1 with a mutual inductance of M, a primary and a secondary self-inductance both of L is designed. The relation between M and L is $M=L\times k$, where k stands for the magnetic coupling coefficient. The concepts of transformer peaking and design details are discussed as follows.

It has been shown that an inductor can generate a zero in frequency domain, cancel the dominant pole, and therefore increase the circuit bandwidth [1]-[3]. Multiple inductors can be employed for further bandwidth enhancement. In our design, a peaking transformer TF1 is used instead of two peaking inductors to gain an additional mutual inductance and consume a smaller chip area. To simplify the metal layer routing and reduce the redundant interconnects, the configuration chosen in this design is Frlan-style transformer [5]. For high mutual inductance of the transformer, k is an important design parameter. The k factor is mainly limited by the minimum metal spacing, which is 1.5 μm in this technology. The simulated k for a 2.5-turn transformer is around 0.64 with a metal width of 15 μm, and a top metal layer thickness of 2 μm. For a higher k, the mutual inductance increases as well as the peaking effects. However, one must pay attention to the design to prevent the over peaking possibility. It was found that using bandwidth enhancement by transformers, due to the excess mutual inductance, can easily cause a gain overshoot characteristic. For example, with a design of L= 2.2 nH, the circuit bandwidth can be improved by ~ 16% when k varies from 0 to 0.64, however, a 4-dB gain overshoot peak is also observed. In our design, the minimum spacing is selected for a maximum k value, while the L is carefully adjusted for both bandwidth enhancement and gain flatness. Due to the mutual inductance in a transformer, L can be reduced to reach an excellent peaking performance with a relatively smaller inductive component area.

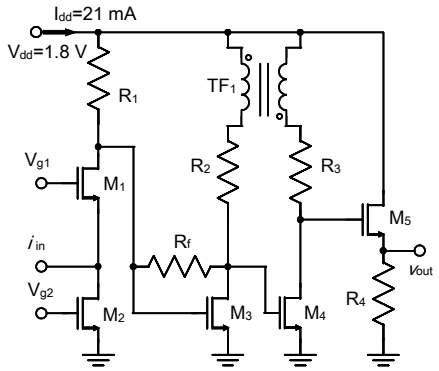

Fig. 1 Schematic of the TIA with transformer peaking.

Fig. 2 compares the simulated effective transimpedance gain (Z_T) of the proposed TIA with different peaking techniques. Case (i) uses a resistive load only topology, which shows a Z_T of 50 dBΩ and a 3-dB bandwidth of 3.5 GHz. Case (ii) employs two peaking inductors each of 2.2 nH. The 3-dB bandwidth is 6.1 GHz with a maximally-flat frequency response. The bandwidth has been improved by a factor of 1.7 in case (ii) due to the inductor peaking. Case (iii) shows the result of using a peaking transformer in the circuit. A transformer with two equal self-inductances of

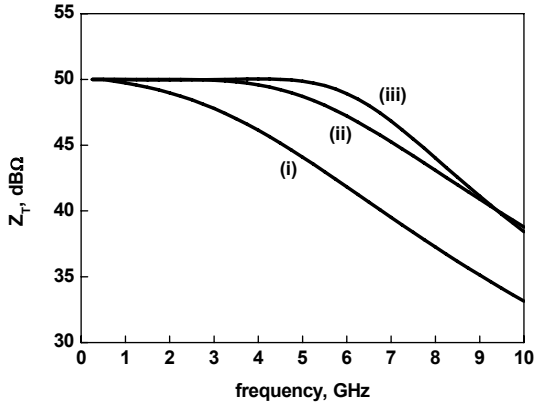

Fig. 2 Simulated Z_T verses frequency for the TIA with (i) resistive load (ii) inductor peaking (iii) transformer peaking.

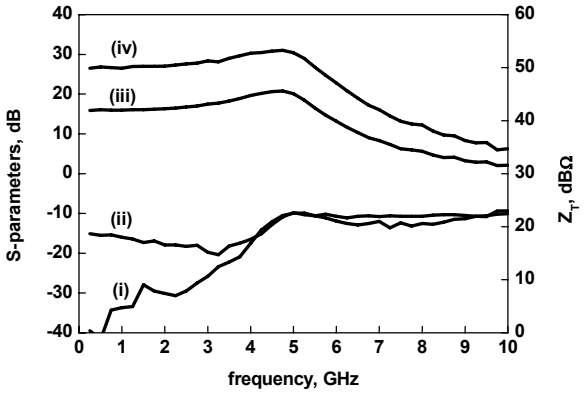

Fig. 3 Measured (i) S_{11}, (ii) S_{22}, (iii) S_{21}, and (iv) Z_T of the TIA.

1.6 nH and a *k* factor of 0.64 is employed for an compromise between bandwidth and gain overshoot. The simulated result shows a 3-dB bandwidth of 7.0 GHz, which increases the bandwidth by a factor of 2.0 compared to that in case (i). Note that, for either the inductors peaking or the transformer peaking cases, the low-frequency gains are not disturbed since the inductive components are essentially short-circuited at low frequencies. In addition, it was found that the optimized self-inductance of a transformer (1.6 nH) in case (iii) is lower than the peaking inductance (2.2 nH) in case (ii). The smaller inductance needed for the transformer peaking technique can further reduce the chip area and achieve a better quality factor for the peaking components.

3. Measured Results

The S-parameters and eye-diagram of the TIA are measured on-wafer with coplanar ground-signal-ground (GSG) probes. Fig. 3 shows the measured S-parameters and Z_T. The low-frequency magnitude and the 3-dB bandwidth of S_{21} are 15.9 dB and 6.0 GHz, respectively. S_{11} is lower than -9.9 dB up to 9.5 GHz, and S_{22} is lower than -9.8 dB

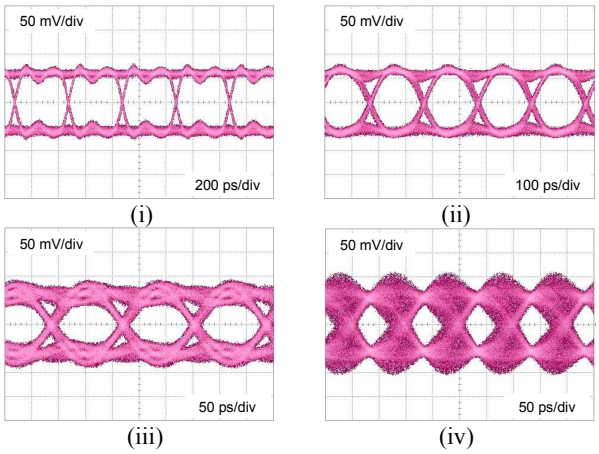

Fig. 4 Measured eye-diagram for 2^{31}-1 PRBS at a bit rate of (i) 2.5-, (ii) 5.0-, (iii) 7.5-, and (iv) 10.0-Gb/s.

up to 10 GHz. The results indicate that a good input/output matching is achieved within the circuit bandwidth. The overshoot in S_{21} may result from an underestimation of the self-inductance and the coupling coefficient of the peaking transformer in our design. The 3-dB bandwidth and the low-frequency Z_T are 6.0 GHz and 50.0 dBΩ with a flatness of 3.1 dB, respectively. The measured Z_T is close to the simulated result, while the bandwidth is lower than the simulated result by about 1 GHz. The difference may be attributed to the inaccuracy of the active device high frequency models.

Fig. 4 displays the measured eye diagram at four different bit rates of 2.5-, 5.0-, 7.5-, and 10.0-Gb/s for 2^{31}-1 pseudo-random binary sequences (PRBS). The measured eye diagram shows an output voltage swing of ~ 100.0 mV_{pp} with a Z_T of 316 Ω (50.0 dBΩ) up to 10.0-Gb/s as an input current swing of 315 μA_{pp}. Ringing in the eye diagram may due to the gain overshoot at near the 3-dB bandwidth frequencies. The TIA consumes 37.8 mW under a single power supply of 1.8 V.

4. Conclusions

A TIA with a peaking transformer using 0.18-μm CMOS technology is reported. The simulated results show that the TIA with a peaking transformer enhances the circuit bandwidth by a factor of 2.0 compared to that with only resistive loads. In addition, the transformer-peaking TIA consumes a smaller chip area than that with two peaking inductors. The presence of mutual inductance in transformers enhances the circuit bandwidth effectively for wideband CMOS TIA design.

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