40-Gb/s Transimpedance Amplifier in 0.18-μm CMOS Technology

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***Abstract*—A 40-Gb/s transimpedance amplifier (TIA) is realized in 0.18-μm CMOS technology. From the measured S-parameters, a transimpedance gain of 51.0 dBΩ and a 3-dB bandwidth up to 30.5 GHz (~ 0.5 f_T) were observed. To the best of authors' knowledge, the TIA presents the widest bandwidth and highest GBP/P_{dc} of 180.1 GHzΩ/mW among the published results with similar technologies. A new bandwidth enhancement technique, π-type inductor peaking (PIP), is proposed, which gives a bandwidth enhancement factor of 3.31 without disturbing the low-frequency gain. Under a 1.8 V supply voltage, the TIA consumes 60.1 mW with a chip area of 1.17 × 0.46 mm^2.**

I. INTRODUCTION

The rapidly increased demands for large data capacity has pushed the data rate of optical communication system from 10-Gb/s (OC-192) up to 40-Gb/s (OC-768) [1]-[4]. For optoelectronic integrated-circuits (OEICs) with such a high operation speed, the design for low cost, low power consumption, high yield, and high integration level become a real challenge. The CMOS-based technology is probably the best candidate to achieve this goal. However, the capability of high operation speed for the wideband circuits is seriously limited by the inherent capacitances in a MOS transistor.

A simple approach to improve the circuit bandwidth is shunt peaking, which introduces an inductor to resonate with the capacitances and gives a bandwidth enhancement factor of 1.85 [5]. Two more effective design techniques are T-coil peaking [6] and shunt-series peaking [4] with the enhancement factors of 2.82 and 3.46, respectively. However, the factors were calculated under certain assumptions, which may not be practical in real circuits. For example, the drain capacitance was neglected for T-coil peaking and the ratio of the gate to drain capacitances was set to be one for shunt-series peaking. Discrepancies between the real circuit and the assumptions may degrade the expected circuit bandwidth.

In this paper, a new wideband technique, π-type inductor peaking (PIP), is proposed to break the bandwidth limitation by resonating with the intrinsic capacitances of the devices. Composed of three inductors, PIP can significantly enhance the bandwidth of a common-source (CS) stage by a factor of 3.31 without disturbing the low-frequency gain. A TIA is realized in the 0.18-μm CMOS technology to demonstrate this design approach. With such an advanced wideband technique, the proposed TIA presents a transimpedance gain (Z_T) of 51.0 dBΩ and a bandwidth of 30.5 GHz (~ 0.5f_T). Compared to the TIAs published recently with 0.18-μm technologies [7]-[9], as summarized in Table I, the CMOS TIA designed by the PIP technique show the highest bandwidth and also the highest gain-bandwidth-product per DC power figure-of-merit (GBP/P_{DC}).

Section II describes the design concept of the proposed PIP technique in a CS stage. A CMOS TIA using four cascaded CS stages with PIP configuration is presented in

Table I
SUMMARY OF THE STATE-OF-THE-ART TIA PERFORMANCES

Ref.	BW (GHz)	Speed (Gb/s)	Z_T (dBΩ)	S_{22} (dB)	$i_{n,in}$ (pA/√Hz)	C_{pd} (fF)	Chip area (mm^2)	V_{DD} (V)	Power (mW)	GBP/P_{dc} (GHzΩ/mW)	Technology
[7]	9.2	10	54.0	—	17.0	500	0.8 × 0.8	2.5	137.5	33.5	0.18-μm BiCMOS
[8]	7.2	10	61.0	—	8.2	250	0.14	1.8	70.2	115.1	0.18-μm CMOS
[9]	9.0	10	62.3	-10.0	—	150	—	1.8	108.0	108.6	0.18-μm CMOS
This work	30.5	40	51.0	-10.0	34.3	50	1.17 × 0.46	1.8	60.1	180.1	0.18-μm CMOS

This research was supported in part by the NTHU-TSMC Joint-Development Project and the National Science Council under Contracts NSC 94-2752-E-007-002-PAE.

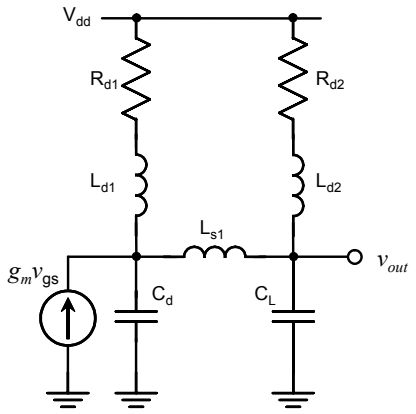

Fig. 1. The small-signal circuit model for a common-source (CS) stage with π-type inductor peaking (PIP) inductors (L_{d1}, L_{s1}, and L_{d2}).

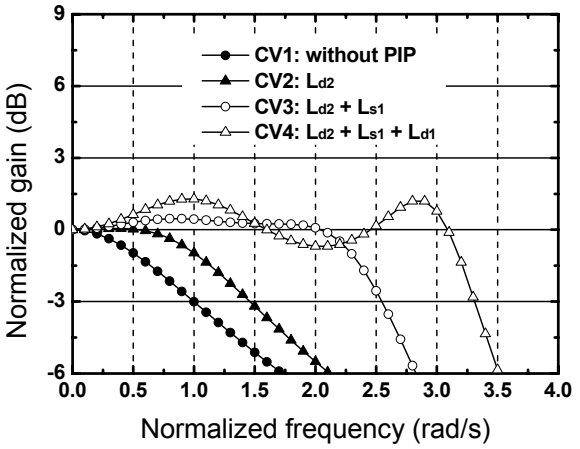

Fig. 2. Progressive bandwidth improvement by each PIP inductor.

section III. The measured results are shown in section IV, and section V concludes this work.

II. π-TYPE INDUCTOR PEAKING (PIP)

The concept of PIP design technique is illustrated by a CS stage first in this section, which is the fundamental building block and will be applied directly to the proposed wideband TIA using a four-stage cascade configuration. Fig. 1 shows a simplified small-signal equivalent circuit model of a CS stage including the PIP inductors (L_{d1}, L_{s1}, and L_{d2}), where C_d is the equivalent drain capacitance, C_L is the equivalent input capacitance from the next stage, and R_{d1} and R_{d2} are the drain resistors. The progressive bandwidth improvement of a CS stage by adding each peaking inductor is described as follows.

Without the peaking inductors, the drain current $g_m v_{gs}$ flows into C_d, C_L, R_{d1}, and R_{d2}, and generates the output voltage v_{out}. The 3-dB bandwidth (ω_0) is limited by the resistive and capacitive loads under this condition. By inserting L_{d2} in series with R_{d2}, the bandwidth is increased by a parallel resonance with C_d and C_L. If L_{s1} is also employed, the bandwidth can be further enhanced by a series resonance with C_L at higher frequencies, which forces more current $g_m v_{gs}$ to flow through L_{s1} and reach the output terminal. Finally, by introducing one more inductor L_{d1}, the rest of the capacitances can be resonated in parallel with L_{d1} to obtain an ultra-wide bandwidth. Based on the circuit shown in Fig. 1, Fig. 2 plots the frequency response of the above four conditions, where ω_0 and the DC gain are normalized, and R_{d1} and R_{d2} are set to be equal. In addition, the ratio of C_L to C_d is set to be three, which is a more practical assumption in the 0.18-μm CMOS technology [10]. The gradually improved bandwidth can be observed as adding the three peaking inductors step by step.

To obtain a more comprehensive understanding of the frequency response, the transfer function $H_{PIP}(s)$ of Fig. 1 is derived as:

$$H_{PIP}(s) = R_{d1}R_{d2}\frac{1+s\left(\frac{L_{d1}}{R_{d1}}+\frac{L_{d2}}{R_{d2}}\right)+s^2\frac{L_{d1}}{R_{d1}}\frac{L_{d2}}{R_{d2}}}{D_0+sD_1+s^2D_2+s^3D_3+s^4D_4+s^5D_5} \quad (1)$$

where

$$D_0 = R_{d1}+R_{d2}$$
$$D_1 = L_{d1}+L_{d2}+L_{s1}+R_{d1}R_{d2}(C_d+C_L)$$
$$D_2 = (C_d+C_L)(R_{d1}L_{d2}+R_{d2}L_{d1})+R_{d1}L_{s1}C_d+R_{d2}L_{s1}C_L$$
$$D_3 = L_{d1}C_d(L_{d2}+L_{s1})+L_{d2}C_L(L_{d1}+L_{s1})+R_{d1}R_{d2}L_{s1}C_dC_L$$
$$D_4 = L_{s1}C_dC_L(R_{d1}L_{d2}+R_{d2}L_{d1})$$
$$D_5 = L_{d1}L_{d2}L_{s1}C_dC_L$$

As can be observed, two zeros (R_{d1}/L_{d1} and R_{d2}/L_{d2}) and two pairs of complex conjugate poles exist in $H_{PIP}(s)$. By an appropriate design, both zeros and complex poles can be employed to enhance the bandwidth. Since the low-frequency gain is determined by the resistances and the capacitances, the remaining design parameters for bandwidth improvement are the inductances. With only L_{d2}, $L_{d2}+L_{s1}$, and $L_{d2}+L_{s2}+L_{d1}$, the transfer functions under different circuit topologies can be derived to find the required inductances for an optimized bandwidth. Based on the equations, the required inductances can be obtained as $a_1 \times R_{d1}^2 \times C_d$, where a_1 for L_{d2}, L_{s1}, and L_{d1} are 1.50, 0.86, and 0.80, respectively. By using above inductances, the bandwidth can be enhanced up to $3.31\times\omega_0$ with a gain flatness within 2.0 dB, as the curve CV4 shown in Fig. 2.

III. DESIGN OF 40-GB/S TIA

To demonstrate the proposed PIP technique, a TIA targeting at 40-Gb/s is realized in 0.18-μm CMOS technology. The 40-Gb/s TIA composes of four cascaded CS stages, as shown in Fig. 3. Identical resistances for the drain basing resistors (R_d) of each stage are employed, and the input and output impedance are both matched to 50 Ω through the matching resistors (R_M). To design for a large gain, a large R_d is preferred. However, the required peaking inductances for PIP topology, as derived in section II, are

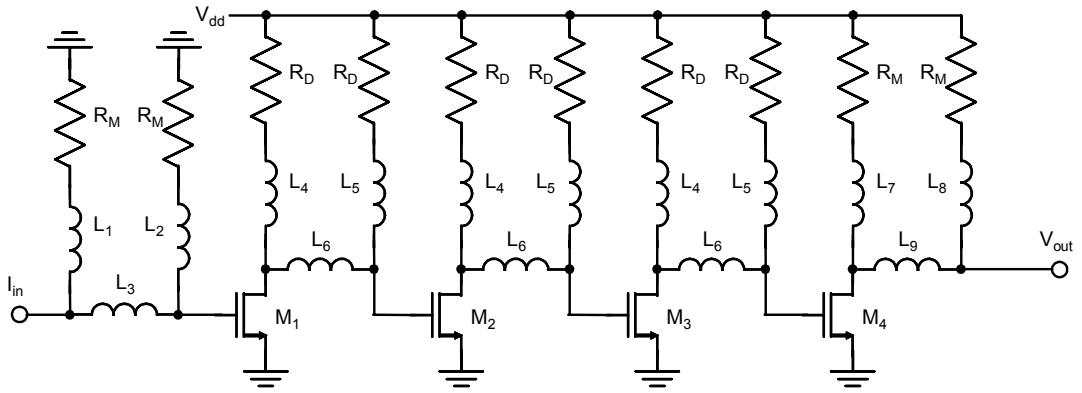

Fig. 3. Circuit topology for the TIA with the PIP technique for bandwidth enhancement.

proportional to R_d^2. It can be seen that a trade-off exist here since a large inductor not only occupies a large chip area but also causes difficulties to maintain inductive up to the circuit bandwidth. The optimized R_d obtained for reasonable inductances, while still with a high gain performance is 200 Ω. The adopted device width of $M_1 \sim M_3$ is 48 μm with a f_T of about 60 GHz, while a larger width of 64 μm is employed for M_4 to increase the gain and driving capability of the output stage. The inductances ($L_1 \sim L_9$) are designed based on the derived transfer functions, while some optimizations are essential due to the frequency dependence of C_d and C_L. It is worth to point out that the parasitic capacitance (C_{pd}) of a photodiode, which is also a main limitation for the TIA bandwidth, can be effectively resonated by the PIP configuration.

The input-referred noise current $\langle i^2_{n,in} \rangle$ is also an important consideration for the TIA design, which is determined by the resistor thermal noise, the drain thermal noise, and the induced gate noise. For MOS transistors with a gate length of 0.18-μm, the measured results indicates that the drain thermal noise dominates the active device noise characteristics [11]-[12]. Therefore, the $\langle i^2_{n,in} \rangle$ for the circuit shown in Fig. 3 can be simplified as:

$$\left\langle i_{n,in}^2 \right\rangle = \frac{8kT}{R_M} + \frac{4kT\gamma}{g_{m1}}\left(\frac{4}{R_M^2} + \omega^2 \left(C_{g1} + C_{gd1} \right)^2 \right) \tag{2}$$

where γ is the coefficient of the drain thermal noise, g_{m1} is the transconductance of M_1, and C_{gd1} is the capacitance between the gate and drain terminals of M_1. Since R_M is designed for the input matching, g_{m1} can be increased to minimize $\langle i^2_{n,in} \rangle$ by either enlarging the drain current or increasing the gate width. Note that the second method also increases C_{g1} and C_{gd1}, which may result in a higher $\langle i^2_{n,in} \rangle$ and a reduced bandwidth.

In addition to the above discussed design issues, the layout of the circuit plays a critical role in the overall circuit performance. For circuits operated in such a high frequency, the signal integrity can be severely suffered from the lossy Si substrate and the crosstalk from adjacent interconnects. In this design, grounded coplanar waveguide (GCPW) configuration of the transmission lines is employed to prevent such problems [13]. The sidewall and bottom ground planes are utilized for a perfect shielding of the signal paths. The TIA was fabricated in 0.18-μm CMOS technology with an area of 1.17 mm × 0.46 mm, as shown in Fig. 4. The GCPW layout can be seen from a large ground metal plane on the surface of the chip photograph.

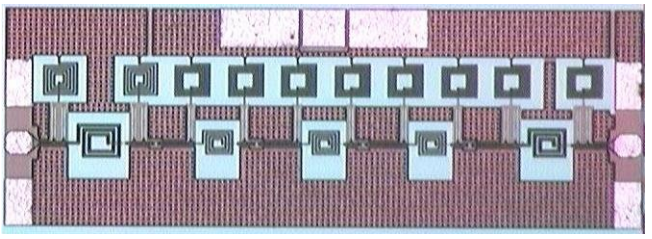

Fig. 4. Chip photograph. (area: 1.17 × 0.46 mm^2)

IV. Measurement Results

The TIA was measured on-wafer with coplanar ground-signal-ground (GSG) probes for S-parameters and noise figure. The measured responses of Z_T are depicted in Fig. 5 and Fig. 6. The gain and the 3-dB bandwidth ($f_{3\text{-}dB}$) are 51.0 dBΩ and 30.5 GHz in the presence of a C_{pd} of 50 fF at the input, respectively, and the phase is very linear as a function of frequency up to 26.0 GHz. The measured S_{22} within the $f_{3\text{-}dB}$ is all below -10 dB, and S_{21} at low frequencies is up to 16.7 dB, as shown in Fig. 7. From the measured noise figure, the extracted $\langle i^2_{n,in} \rangle$ is 34.3 pA/√Hz at 26.0 GHz. Under a 1.8 V supply voltage, the amplifier consumes 60.1 mW. Moreover, an excellent gain-bandwidth-product per DC power figure-of-merit of 180.1 GHzΩ/mW (GBP/P_{dc}) is obtained. The circuit performances of the 40-Gb/s TIA is summarized in Table I together with the state-of-the-art 0.18-μm CMOS TIAs published recently. Among them, the proposed TIA features the highest bandwidth and the smallest power consumption with the similar technologies.

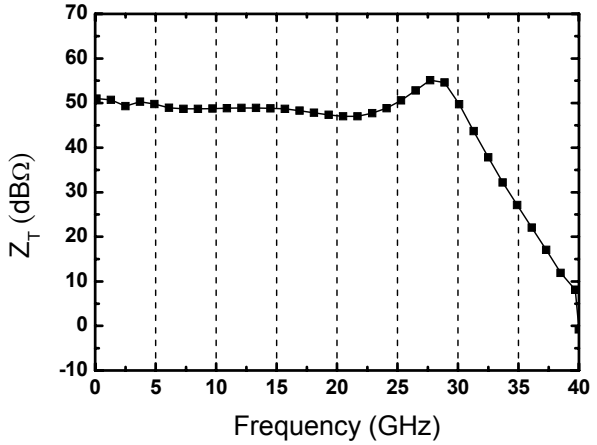

Fig. 5. Measured result of Z_T (magnitude) for the 40-Gb/s TIA in a 0.18-µm CMOS technology.

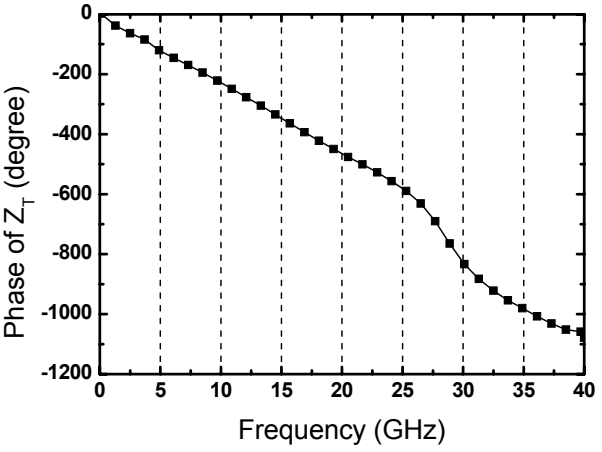

Fig. 6. Measured result of Z_T (phase) for the 40-Gb/s TIA in a 0.18-µm CMOS technology.

V. CONCULSION

In this paper, a newly proposed bandwidth improvement technique has been demonstrated. The PIP technique can enhance the 3-dB bandwidth of a CS stage by a factor of 3.31 without disturbing the low-frequency gain. A 0.18-µm CMOS TIA was realized to demonstrate this approach. From the measured results, the proposed TIA presents the highest bandwidth of 30.5 GHz to date with 0.18-µm CMOS technology. In addition, an excellent gain-bandwidth-product per DC power figure-of-merit of 180.1 GHzΩ/mW (GBP/P_{dc}) was obtained.

ACKNOWLEDGMENT

The authors would like to thank National Chip Implementation Center (CIC) and TSMC both for the chip fabrication. We also like to thank Mr. Chih-Yuan Chan for the chip measurement and Prof. C.S. Chang for support of this work.

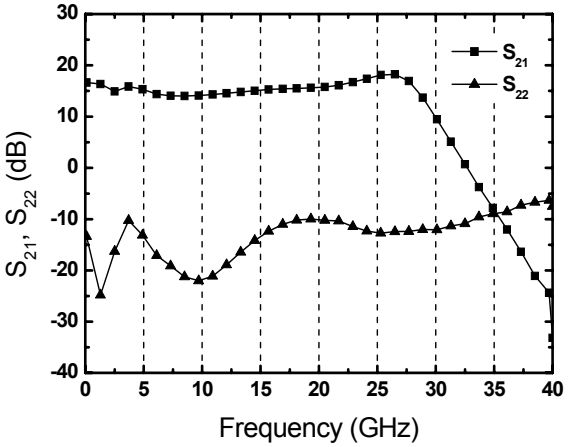

Fig. 7. Measured results of S_{21} and S_{22} for the 40-Gb/s TIA in a 0.18-µm CMOS technology.

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