A Low-Power Low-Noise Amplifier for K-Band Applications

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***Abstract*—This study presents a high performance K-band low noise amplifier. By utilizing transformer feedback at the input stage, an excellent noise figure (NF) of 4.3 dB is obtained at 22 GHz. With the current-reused technique between the two stages, the amplifier achieves a maximum power gain of 10.1 dB under a supply voltage of 1.8 V and a power consumption of only 7.2 mW. The proposed LNA has comparable NF and gain, while it can operate under the lowest power among the published works in 0.18 μm CMOS technology for K-band applications.**

***Index Terms*—Current-reused, low noise amplifier (LNA), noise figure (NF), transformer feedback.**

I. Introduction

CMOS technology is attractive due to its high-level integration for SOC (system-on-chip) applications. Recently, the demand for higher data rates has increased the desired operation frequency of RFICs. Among these applications, K-band (18–26.5 GHz) is of great interest to both industry and academia for short-range and high data-rate wireless communications and anti-collision radars [1].

In this study, we propose a low noise amplifier (LNA) for K-band applications using a standard 0.18 μm CMOS technology. Being the first block of the receiver chain in the transceiver, the LNA plays a crucial role in amplifying the input signal. The design challenge is to achieve low noise figure (NF) and high gain simultaneously while maintaining low power consumption. In this work, an on-chip transformer is adopted as the input matching network for better noise and power matching. The current-reused configuration is also used to reduce the power consumption. In addition, the grounded-coplanar-waveguide (GCPW) structure is employed in the layout to further reduce the signal loss and undesired noise coupling [2]. With these techniques, a K-band transformer feedback LNA demonstrates an excellent NF of 4.3 dB with a power gain of 10.1 dB while consuming only 7.2 mW.

II. Circuit Topology and Analysis

Fig. 1 shows the proposed CMOS K-band transformer feedback LNA utilizing the current-reused technique. As can be seen, a transformer is employed as the input matching network, and the inter-stage network composed of the inductor L_D and the capacitor C_G performs a current-reused function to achieve high power gain under low power consumption. Inductor L_L functions as inductive peaking for operation frequency enhancement. The output matching network is constructed by the capacitors C_{D2} and C_{M1}. Note that C_{D2} is also used as the ac coupling capacitor to block the dc current.

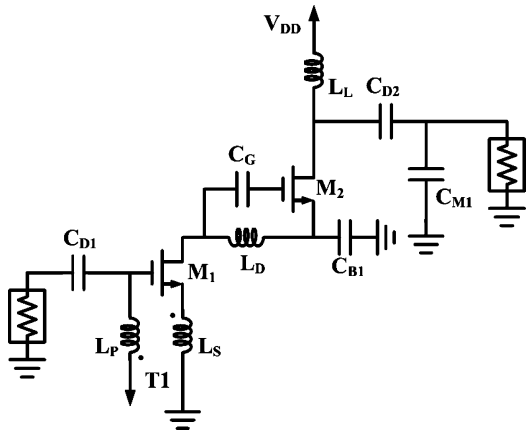

Fig. 1. Schematic of the proposed current-reused LNA.

A. Transformer Feedback Matching Network

In this letter, the input matching network is designed by a transformer together with an ac coupling capacitor C_{D1}. The primary coil in the transformer is connected in parallel to the gate of M_1, and the secondary coil is connected in series to the source as shown in Fig. 1. Compared with the two individual spiral inductors usually used for LNA design [2] (one gate inductor and one source inductor), the transformer occupies less chip area and exhibits a higher quality factor. The insertion loss of the input matching network is thus reduced and a smaller NF can be expected.

In addition, the transformer feedback design offers advantages of improved gain, stability, and particularly the noise and power matching capability for LNA [3]. As shown in Fig. 1, the secondary coil L_S acts as inductive degeneration in the common-source stage $M1$, resulting in a real impedance for better matching to 50 ohm. The primary coil L_P at the input node also provides the flexibility to further match the imaginary part. Finally, the high coupling factor of the transformer can reduce the effect of channel noise of M_1 on NF and the flatness of NF in the desired bandwidth can also be improved [4]. With EM simulation, the optimized values in the final design for L_S

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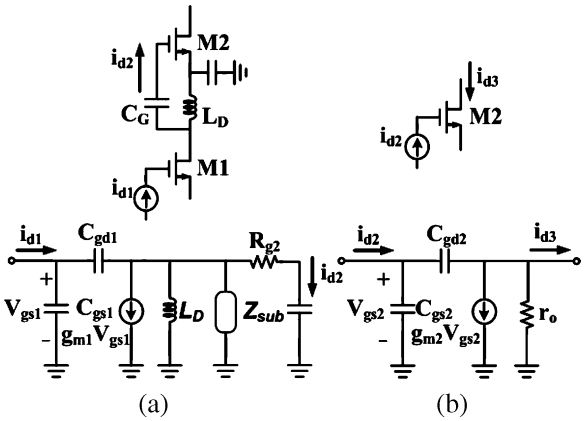

Fig. 2. Current-amplifying characteristics of (a) input stage (b) second stage.

and L_P are 70 and 220 pH, respectively and the coupling factor is about 0.4 at the desired operation frequency.

B. Current-Reused Technique

The current-reused stage includes the transistors M_1, M_2, the inductor L_D, and the capacitors C_G and C_{B1}. The purpose of using C_G is to create a low impedance path without any dc current, while the impedance of L_D increases with frequency leading to a high impedance path to block the signal. As a consequence, the input signal can be amplified twice under this con-current structure. With this design technique, a high gain can be obtained under a low dc power consumption. Note that a large C_G is preferred in the design for a better signal coupling. However, a large MIM capacitor may suffer from the parasitic capacitances between the bottom plate and the substrate, which could degrade the circuit performance. In this case, the optimized value of C_G is about 20 fF and L_D is about 330 pH.

Fig. 2 shows the conceptual current-reused scheme in our design. Fig. 2(a) is the input stage, where Z_{sub} represents the parasitic impedance comprising transistor M_1's drain parasitic capacitance in series with the effective substrate resistance R_{sub}. C_{in} is the equivalent capacitance composed of C_G and C_{gs2} of M_2. At high frequencies, the MOS transistor acts as a current amplifier, and the current-amplifying characteristic of the first stage can be derived. The current gain i_{d2}/i_{d1} can be expressed as follows:

$$\frac{i_{d2}}{i_{d1}} = \frac{g_{m1}}{s(C_{gs1}+C_{gd1})} \cdot \frac{sL_D//Z_{sub}}{sL_D//Z_{sub}+R_{g2}+\frac{1}{sC_{in}}} \approx \frac{g_{m1}}{s(C_{gs1}+C_{gd1})}. \quad (1)$$

Note that (1) is based on an assumption that $sL_D//Z_{sub}$ provides a sufficiently high impedance along the signal path. From Fig. 2(b), the current gain i_{d3}/i_{d2} can be obtained as

$$\frac{i_{d3}}{i_{d2}} \approx \frac{g_{m2}}{s(C_{gs2}+C_{gd2})}. \quad (2)$$

Combining (1) and (2), it can be seen that the input signal is amplified twice under the same dc current for achieving high gain under low power consumption.

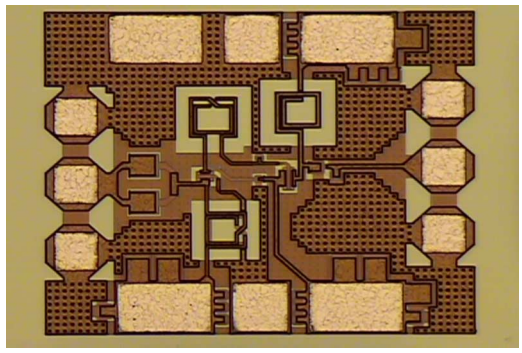

Fig. 3. Micrograph of the proposed LNA. ($\mathrm{Core\ size} = 0.4 \times 0.32\ \mathrm{mm}^2$).

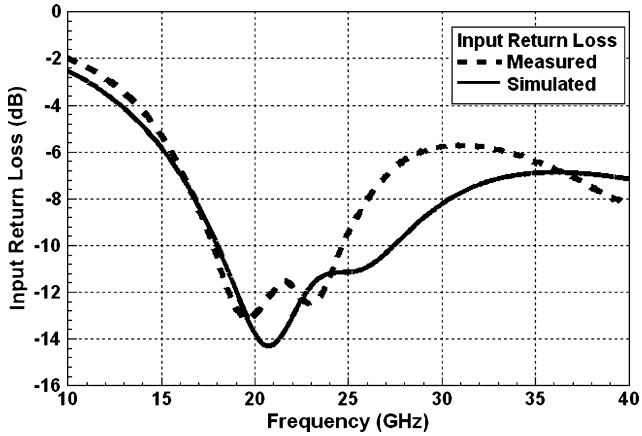

Fig. 4. Measured and simulated input reflection coefficients.

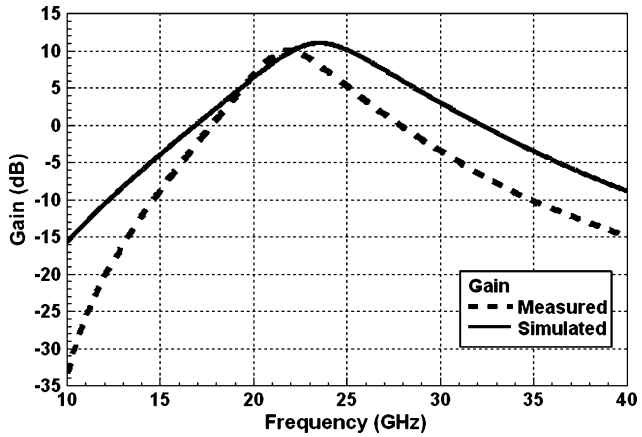

Fig. 5. Measured and simulated power gains.

C. Layout Consideration

For circuits operating at high frequencies, layout becomes a critical issue for the overall circuit performance. The grounded-coplanar-waveguide (GCPW) configuration is employed for the transmission lines [2]. In our design, Metal 1 is used as the ground plane and Metal 6 is used as the signal line. Besides, the signal line is surrounded by other metal layers connected through the vias. As a result, signal loss can be reduced and interference from the substrate coupling can be alleviated. Note that the similar approach is adopted for the guard rings of the inductors and transformers. With all the metal layers connected

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PUBLISHED WORKS

Specification	*This work*	[5]	[6]	[7]	[8]
Technology (CMOS)	0.18 μm	0.18 μm	0.18 μm	0.18 μm	90 nm
Peak gain frequency (GHz)	22.0	23.7	24.0	21.8	20
Power gain (dB)	10.1	12.8	13.1	15	5.8
Noise figure (dB)	4.3	5.6	3.9	6	6.4
P_{diss} (mW)	7.2	54	14	24	10
Input return loss (dB)	12	11	15	21	11
IIP3 (dBm)	-1	+2	0.5		
Supply voltage (V)	1.8	1.8	1	1.5	1.5

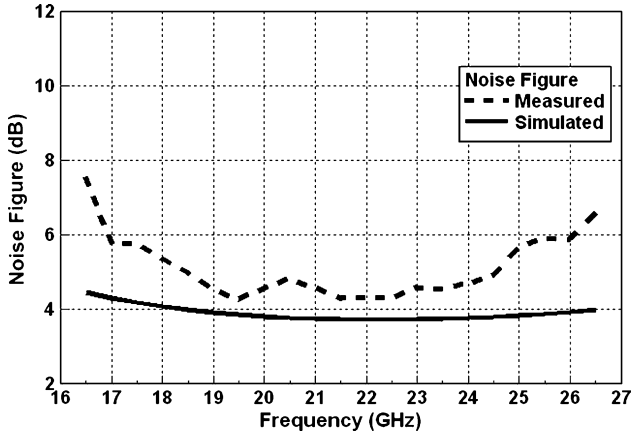

Fig. 6. Measured and simulated NFs.

by the vias to form the guard rings, the undesired coupling effect between the inductive components and the signal lines can be improved.

III. MEASURED RESULTS

Fig. 3 shows the microphotograph of the fabricated LNA and Fig. 4 presents the measured and simulated input reflection coefficients. The total dc power consumption is only 7.2 mW under a 1.8 V power supply. As can be seen, low S_{11} values of a relatively wide bandwidth (~6.8 GHz, below −10 dB) demonstrate a successful design of using the on-chip transformer as the input matching network. Fig. 5 shows the measured and simulated power gains as a function of frequency. The two curves are in a good agreement and the measured power gain is 10.1 dB at 22.0 GHz. Fig. 6 compares both the measured and simulated NFs. The result shows an excellent noise performance of 4.3 dB at 22.0 GHz. In addition, the NF is below 4.8 dB within the 3-dB bandwidth (~4.1 GHz), which also indicates the input transformer is suitable for wideband low noise design. Under the same bias condition, the measured input-referred 1-dB compression point and IIP3 are −10 dBm and −1 dBm, respectively. Table I summarizes the performance of recently published K-band LNAs by standard 0.18 μm CMOS technology [5]–[8]. As can be seen, the proposed LNA has comparable NF and gain while consuming lowest power among the published results.

IV. CONCLUSION

A low-power low-noise amplifier for K-band applications was demonstrated using 0.18 μm CMOS technology. By employing the on-chip transformer, a well-matched input stage for both noise and gain was achieved. In addition, the current-reused inter-stage reduced the power consumption effectively. The proposed LNA showed a peak power gain of 10.1 dB, NF of 4.3 dB and a wideband input matching under a power consumption of only 7.2 mW.

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