STI Effect on Flicker Noise in 0.13-μm RF NMOS

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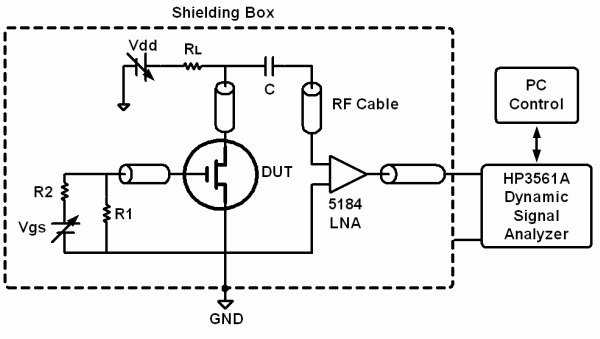
***Abstract*—This paper reports the effect of shallow-trench-isolation (STI) on generation-recombination (G-R) noise and flicker noise variation in 0.13-μm RF MOSFETs for the first time. The devices with relatively small finger widths (W= 1 μm/N_{finger}= 40 and W= 5 μm/N_{finger}= 8) presented more pronounced G-R noise compared to those with W= 10 μm/N_{finger}= 4 devices. In addition, a wide variation of noise levels was observed for devices with smaller finger widths and more finger numbers. The results can be explained by the effect of STI, which affects the carrier mobility due to the compressive stress, also generates traps at the edge of STI region resulting in G-R noise. Moreover, the metals employed in 0.13-μm CMOS technology, Cu and Co, may also be responsible for the G-R noise observed in the devices.**

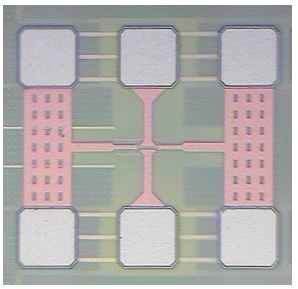
I. INTRODUCTION

The impact of STI on MOSFET characteristics has been studied and the distance between the edges of shallow-trench-isolation (STI) to the gate has been demonstrated to play an important role in the device DC characteristics [1]-[3]. The mechanical stress introduced by STI and stress-control layers on flicker noise in CMOS has also been studied previously [4]-[5]. Flicker noise of MOS transistors mainly results from the traps/interface states in the devices, which can be a crucial factor in the performance of nonlinear RFICs such as voltage controlled oscillators (VCOs) and mixers [6]. Studies focused on noise origins and modeling for advanced CMOS technologies were also published [8]. However, little has been reported regarding the impact of STI induced stress and traps on flicker noise. Neither detailed study on the physical origins nor the G-R noise of devices was discussed.

In this study, the flicker noise characteristics of 0.13-μm RF N-MOSFETs with a fixed total width but various finger widths and finger numbers are investigated systematically. Many devices of each type from different chips are characterized to obtain a statistical conclusion. The results indicate that STI effect on flicker noise depends strongly on the device geometries. Both mobility fluctuation and carrier number fluctuation play important roles in the observed trends. The compressive stress along the Y-direction results in a profound modulation on carrier mobility for devices with smaller width. On the other hand, the traps existed in the adjacent area of STI and active region interface is a main factor of the pronounced G-R noise. The metals used in advance CMOS technology such as Co and Cu, which can introduce deep-level traps, may also be critical for the appearance of G-R noise. Section II describes the noise measurement setup and the devices layout and structure. Section III presents the experimental results and discussion. Section IV concludes this works.



(a)



(b)

Fig. 1. (a) Flicker noise measurement setup. (b) Photograph of a 0.13 μm RF N-MOSFET with ground-signal-ground (G-S-G) RF pads.

II. FLICKER NOISE MEASUREMENT SETUP AND DEVICES STRUCTURE

Fig. 1(a) shows the setup for flicker noise measurements. A low-noise preamplifier with a noise floor of 6.4 x 10^{-21} V^2/Hz was used to amplify the noise voltage, which is converted from the device drain noise current by R_L. Low-loss RF cables and probes with excellent ground shielding were used for the signal paths. In addition, the devices and the system including the preamplifier and probe station were

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enclosed in a shielding box to further reduce the environmental interference. Moreover, a battery-powered DC voltage source was employed to prevent the additional noise introduced by the power supply. The noise measurements were performed in a range of 10 Hz to 100 KHz, and the noise floor of the system was well below the tested devices in the measured frequency range.

Fig 1(b) shows the layout of the RF MOSFETs with ground-signal-ground (G-S-G) RF pads. For nanometer devices with very high low-frequency gain, using a well-grounded signal path including RF pads and the above mentioned system can effectively avoid the devices oscillation problem during the measurement to obtain reliable results [7]. The gate terminal was AC short-circuited through a large capacitor and the drain current noise spectral density was measured. Devices characterized in this study were fabricated by a standard CMOS 0.13-μm process, with a gate oxide thickness of ~ 27 Å, and a threshold voltage of ~ 0.4 V. Devices with three different finger widths including 1, 5, and 10 μm and the corresponding finger numbers of 40, 8, and 4 were tested, which have the same total channel width of 40 μm for a fair comparison.

III. Results and Discussion

A. DC Characteristics

Five devices of each type on different chip were characterized under various bias conditions to obtain a statistical indication on device properties. Fig. 2 shows the deviation of DC current for devices with different finger widths and numbers. As can be seen, the averaged drain current reduced as the finger number increases. Also, the devices with W= 1 μm (N_{finger}= 40) presented a significantly wider variation than those with W= 5 μm (N_{finger}= 8) and W= 10 μm (N_{finger}= 4). The results can be attributed to the stress effect originated from STI field oxide which can generate non-uniform compression stress especially between the trench edge and the active region. As a result, the STI induced stress can reduce the carrier mobility of electrons in NMOS leading to a reduced drain current [1]-[3]. The results suggest that the devices with a larger finger number (smaller finger width) suffered more from the STI stress effect, which results in a smaller average drain current. Moreover, the devices with more finger numbers are more sensitive to the STI stress variation resulting in a larger distribution in the drain current. More discussions together with the noise characteristics and the dependence of device geometries will be carried out later.

B. Flicker Noise Characteristics

Fig. 3, Fig. 4, and Fig. 5 present the normalized drain noise current spectral density for NMOS devices with W= 1 μm (N_{finger}= 40), W= 5 μm (N_{finger}= 8), and W= 10 μm (N_{finger}= 4), respectively. The gate bias (V_{GS}) varied from 0.5 to 0.8 V under a fixed drain bias (V_{DS}) of 1 V. As can be seen in both Fig. 3 and Fig. 4, the devices present a large

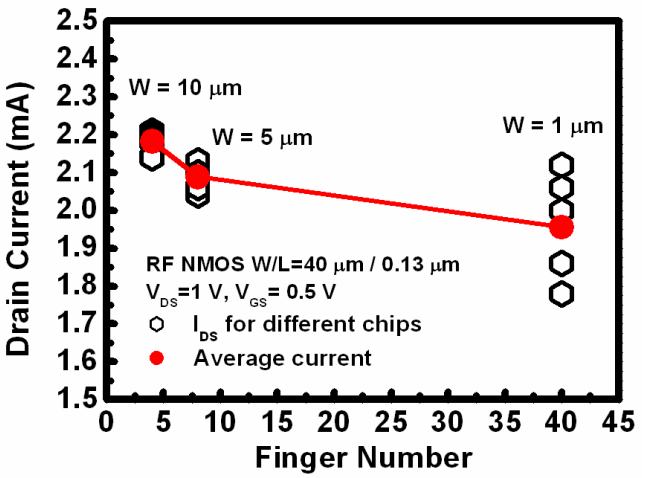

Fig. 2. Drain current variations as a function of finger number for 0.13 μm RF NMOS devices.

variation of the noise level and pronounced G-R noise components. However, a significantly smaller variation of flicker noise was observed for the devices with W= 10 μm/N_{finger}= 4 as shown in Fig. 5.

For a deeper understanding of the observed trends, the unified flicker noise model was employed to explain the experimental results. The unified model can be describes by the following equation [8]:

$$\frac{S_{ID}}{I_{DS}^2} = \frac{kT}{\gamma^{\eta} WL^2} \int_0^L N_t(E_{fn}) \cdot \left[\frac{1}{N(x)} \pm \alpha\mu \right]^2 dx \qquad (1)$$

where N_t is the trap density, α is the scattering parameter, μ is the carrier mobility, N is the carrier density in channel, and γ is the attenuation coefficient of the electron wave function. It can be seen from (1) that both mobility and carrier number fluctuations are the possible origins of flicker noise.

As mentioned, the devices with a smaller W but larger N_{finger} suffered more non-uniform STI stress, which can cause variations of carrier mobility in the channel. According to (1), the carrier mobility has a direct impact on noise characteristics. As a result, the devices present a more obvious variation of noise current spectral densities (more than one order of magnitude) even under the same bias condition. The explanation is consistent with the observed results of the drain DC current variation.

In addition to the mobility variation, the carrier number fluctuation can be responsible for the observed G-R noise. As can be seen, many bulges were observed for devices with a smaller width and more fingers, which are an indication of pronounced G-R noise. For STI process in advanced CMOS technology, due to the stress from lattice mismatched Si and SiO_2 interface, and the damage of the surface and the sidewall introduced by the polish procedure, it is very likely

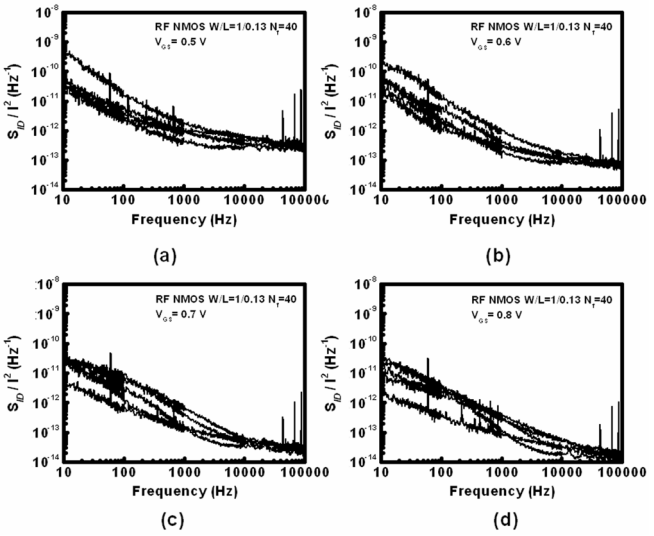

Fig. 3. Noise current spectral density for 0.13-μm RF NMOS with W= 1 μm and N_{finger}= 40 under V_{DS} of 1.0 V and (a) V_{GS}= 0.5 V, (b) V_{GS}= 0.6 V (c) V_{GS}= 0.7 V, (d) V_{GS}= 0.8 V.

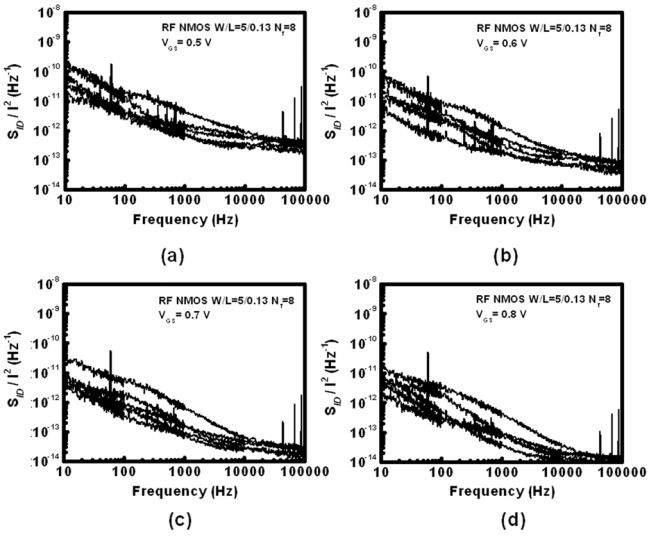

Fig. 4. Noise current spectral density for 0.13-μm RF NMOS with W= 5 μm and N_{finger}= 8 under V_{DS} of 1.0 V and (a) V_{GS}= 0.5 V, (b) V_{GS}= 0.6 V (c) V_{GS}= 0.7 V, (d) V_{GS}= 0.8 V.

that ample traps can be generated especially around the interface of the active region and the STI edge. The measured results suggest that these traps have a higher impact on devices noise characteristics with more finger numbers and a smaller width as well.

Fig. 6 is a conceptual plot of the device layouts to explain the observed trends. The surrounding area is the STI region, and the center is the active region. Two devices with W= 10 μm (N_{finger}= 4) and W= 1 μm (N_{finger}= 40) are shown, where the arrows indicate the directions of the main compression stress in each device. For the device with W= 10 μm, the carriers in the channel should suffer more stress from the X direction than that from the Y direction, while it is the

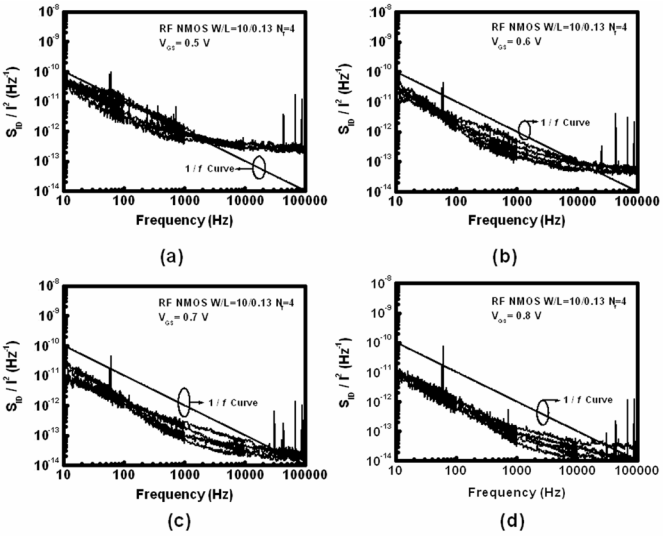

Fig. 5. Noise current spectral density for 0.13-μm RF NMOS with W= 10 μm and N_{finger}= 4 under V_{DS} of 1.0 V and (a) V_{GS}= 0.5 V, (b) V_{GS}= 0.6 V (c) V_{GS}= 0.7 V, (d) V_{GS}= 0.8 V.

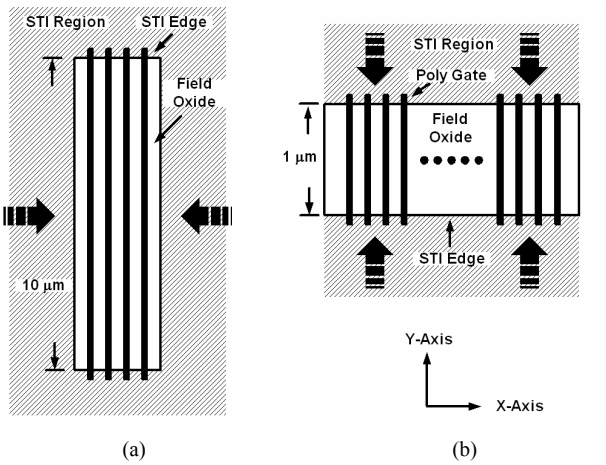

Fig. 6. The device layout for 0.13-μm RF NMOS with (a) W= 10.0 μm and N_{finger}= 4 and (b) W = 1.0 μm and N_{finger}= 40.

opposite condition for the device with W= 1 μm. The measured results suggest that the effect of the X-axis force on a wide device with less finger number is not obvious as can be seen from both the DC and noise characteristics. On the other hand, the effect of STI on devices with W= 1 μm and 40 fingers could be twofold. First, the STI edges in the Y direction are very close to the center of channel, therefore the stress can directly affect the conducting carriers for a mobility reduction and fluctuation. In addition, the sidewall and the edge of the STI have abundant traps, which are also very close to the center of the channel and can also affect the noise characteristics especially the G-R noise components. Therefore, the observed DC current reduction and variation can be mainly attributed to the strong compression stress from STI in the Y direction. In addition, the variations of noise levels are due to both the mobility

fluctuation from the stress and carrier number fluctuation from the traps in the edge of STI and the active region. The pronounced G-R noise should be mainly originated from the structural defects at the edge of STI, since the G-R phenomena often relates to the capture and release of carriers by traps.

Another issue may relate to the observed G-R noise is the metals employed in the advanced CMOS process such as 0.13-μm technology. Since the drain/source metal contacts are very close to the edge of STI (typical distance below 0.1 μm in the technology used here), these metals can penetrate into high stress area between the STI edge and active region during the annealing procedure, which can generate traps relate the donor or acceptor levels of the metals in Si. The corner frequency of the G-R noise can be estimated by the equation shown below [9]:

$$f_{G-R} = \frac{1}{\tau} = \upsilon_0 \cdot \exp\left(-\frac{eE_n}{kT}\right) \qquad (2)$$

where v_o is a vibration frequency, usually in an order of 10^{12} sec^{-1} for Si, E_n is the trap activation energy, k is the Boltzmann constant, and T is the operation temperature.

In advanced CMOS process, both Co and Cu are employed, where the Co silicide is used to improve the contact resistance, and the Cu is used for high-conductivity interconnects. The donor and acceptor levels of these two metals in Si, which can be considered as deep level traps, are listed in Table I. [10]. Based on (2), the calculated corner frequencies of G-R noise are in the range of 100 Hz ~ 1 KHz, which is consistent with the observed results in Fig. 3 and Fig. 4. Compared to the major metal Al employed in 0.18-μm technology, which only has a shallow acceptor level of ~ 0.067 eV in Si, it is likely that the newly introduced metals in 0.13-μm technology is also a reason for observed pronounced G-R noise characteristics.

TABLE I. DONOR AND ACCEPTOR LEVELS OF CU AND CO IN SILICON

	Donor and Acceptor Level (eV)	
	E_c-E_d *(Donors)* eV	E_a-E_v *(Acceptors)* eV
Cu	--	0.53
	--	0.4
	--	0.24
Co	0.53	--
	--	0.49
	--	0.35

Finally, an important finding has to be pointed out is that RF MOS devices for maximized high-frequency performance tend to be design with multifingers with a relatively small finger width to reduce the gate resistance. For example, a 100×1 μm/0.13 μm NMOS transistor has been reported for f_{max} of 135 GHz [11]. However, a large deviation due to the impact of STI effect can be expected in both DC and noise characteristics for such a device design approach based on the above discussion, which can be a serious problem for circuit applications.

IV. CONCLUSIONS

In this study, the impacts of STI on flicker noise in 0.13-μm RF NMOS have been investigated. For devices with the same W/L ratio, the devices with more fingers and a smaller width presented a wide variation in both DC current and noise characteristics. In addition, a pronounced G-R noise was observed in these devices. The results can be attributed by the stress and traps introduced by STI and explained by a unified noise model. The results also indicated that the STI stress has less effect from the X direction for devices with a longer finger width. Moreover, the metals used in advanced 0.13-μm process can introduce deep level traps, which may also be responsible for the G-R noise.

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